

GL4A5/GL5A5 AMD Renoir FP6 Logic Schematics

NM-C741

VER 1.0
March.6.2020

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10.FP6(G)(H) USB/WIFI
11.FP6(I) CAM
12.FP6(J) POWER
13.FP6(K)(L)(M) GND
14.DECAP_VDDCR_VDD MLCC
15.DECAP_VDDCR_SOC MLCC
16.BLANK
17.BLANK
18.BLANK
19.BLANK
20.RTC BATTERY
21.SPI FLASH
22.BLANK
23.RETIMING_PS8818 & TUSB544
24.BLANK
25.BLANK
26.BLANK
27.BLANK
28.BLANK
29.BLANK
30.BLANK
31.BLANK
32.BLANK
33.DDR4 SUB CHANNEL-A
34.DDR4 SUB CHANNEL-A
35.DDR4 SUB CHANNEL-B

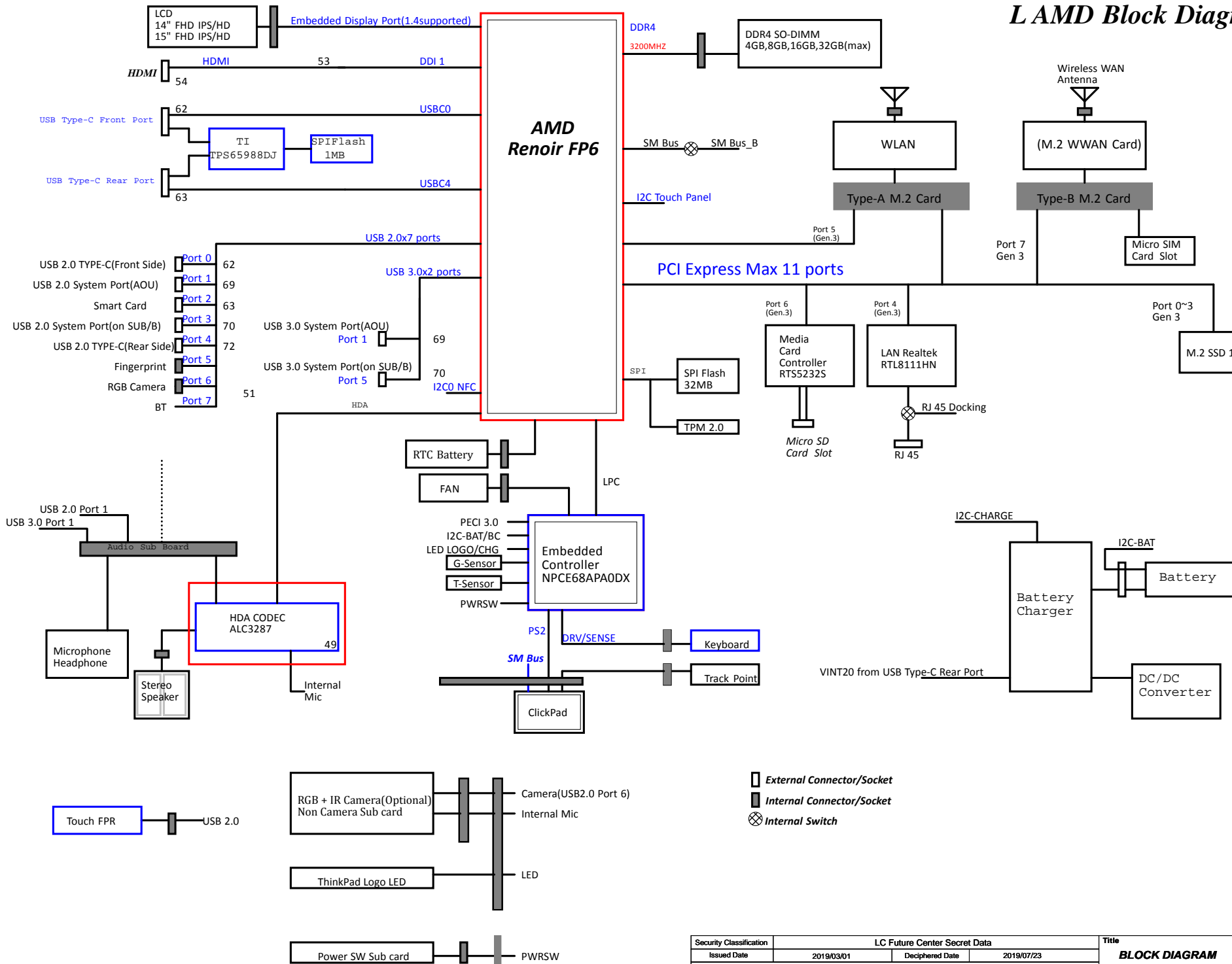
36.DDR4 SUB CHANNEL-B
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43.BLANK
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45.BLANK
46.BLANK
47.BLANK
48.BLANK
49.BLANK
50.BLANK
51.LCD CAMERA/MIC/TOUCH
52.BLANK
53.BLANK
54.HDMI CONNECTOR
55.BLANK
56.BLANK
57.PCIE Re-driver-1
58.PCIE Re-driver-2
59.THUNDERBOLT PD(TPS65988DJ)
60.BLANK
61.USB_HUB_GL852G
62.DOCKING CONNECTOR
63.TYPE-C CONNECTOR
64.M.2 SSD1
65.BLANK
66.M.2 WLAN
67.M.2 WWAN_SOCKET
68.BLANK
69.USB3 AOU CONN
70.BTB_CONN

71.BLANK
72.Smart Card Reader
73.LAN-RTL8111EPV
74.LAN SWITCH
75.LAN_CONNECTOR
76.MEDIA CARD CONTROLLER
77.MEDIA CONNECTOR
78.AUDIO ALC3287
79.BLANK
80.BLANK
81.AUDIO EXIT MIC
82.AUDIO SPEAKER
83.AUDIO BEEP
84.AUDIO DEBUG
85.EC_NPCE68APA0DX(1/2)
86.EC_NPCE68APA0DX(2/2)
87.BLANK
88.KEYBOARD/TRACK POINT
89.TOUCH PAD/NFC/FPR
90.FAN CONNECTOR
91.APS G-SENSOR
92.THERMAL SENSOR
93.BLANK
94.BLANK
95.BLANK
96.BLANK
97.BLANK
98.DISCRETE TPM 2.0
99.SCREW HOLES
100.DC-IN
101.BATTERY INPUT
102.BATTERY CHARGER(BQ25700)
103.DC/DC VCC5M (LV6228C)
104.DC/DC VCC5M_PD(LV6228C)
105.DC/DC VCC3M (SYX198B)


106.DC/DC VCC1R2A(RT8231A)
107.DC/DC VCC2R5A(RT8068A)
108.DC/DC VDDC(LV3667BT)
109.DC/DC VDDC_VDD(RT9610C)
110.DC/DC VDDCR_SOC (RT9610C)
111.BLANK
112.DC/DC Decoupling Cap
113.BLANK
114.DC/DC VDDP0R75(NB691GG)
115.BLANK
116.DC/DC VCC1R8_SUS(NB691)
117.BLANK
118.BLANK
119.BLANK
120.BLANK
121.BLANK
122.BLANK
123.BLANK
124.LOAD SW PCH SUS
125.BLANK
126.BLANK
127.LOAD SW B
128.LOAD SWITCH_+1.8 & 0.75VS

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L AMD Block Diagram



- External Connector/Socket
- Internal Connector/Socket
- Internal Switch

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STATE	SIGNAL	SLP_S3#	SUSP#	SLP_S5#	SYSON	EC_ON	
S0		HIGH		HIGH	ON		
S3 (Suspend to RAM)		LOW		HIGH	ON		
S4 (Suspend to Disk)		LOW		LOW	ON		
S5 (Soft OFF)		LOW		LOW	ON		

USB2 Port

Port	Device
0	Type-C front
1	USB3.0 AOU
2	SMART CARD
3	DB
4	Type-C rear
5	FPR
6	Camera
7	USB HUB

USB3 Port

Port	Device
0	Type-C front
1	Port1 AOU
4	Type-C rear
5	DB

PCIE Port

Port	Device
GPP0~3	SSD1
GPP4	LAN
GPP5	WLAN
GPP6	Card reader
GPP7	X
GPP8~9	WWAN
GFX0~7	X

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	VSYS15	VCC3M VCC5M VCC1R8_SUS VDD0R75	VCC1R2A VCC2R5A	VCC5B VCC3B VCC1R8B +0.75VS_VDDP VCC0R6B VDDCR_SOC VDDC_VDD
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
G3 AC & Battery don't exist	X	X	X	X

SMBUS Control Table

Schematic	SOURCE	TP	LAN	BATT	Charge	HUB	APU	USBC Retime	G-Sensor	Thermal Sensor	SODIMM	CP Module	NFC
SMB03_CLK SMB03_DATA	EC VCC3B	X	X	X	X	X	X	X	V VCC3B	V VCC3B	X	X	X
I2C_CLK_MUX I2C_DATA_MUX	EC VCC3SW_EC	X	X	X	X	X	X	V VCC3_SUS	X	X	X	X	X
I2C_CLK_BT I2C_DATA_BT	EC VCC3SW_EC	X	X	V	V	X	X	X	X	X	X	X	X
SMB0_CLK SMB0_DATA	APU VCC3B	X	X	X	X	X	V VCC3B	X	X	X	V	V	X
SMB1_CLK SMB1_DATA	APU VCC3M	V	V	X	X	V	V VCC3M	X	X	X	X	X	X
I2C0_CLK I2C0_DATA	APU VCC3B	X	X	X	X	X	V VCC3B	X	X	X	X	X	V

PD Controller I2C

	SOURCE	APU	
USBC_PD_I2C_SCL USBC_PD_I2C_SDA	PD VCC3_LDO_PD	V VCC1R8_SUS	
I2C_CLK_TBT I2C_DATA_TBT	PD VCC3_LDO_PD	V VCC3B	
I2C_CLK_PD I2C_DATA_PD	PD VCC3_LDO_PD	EC V VCC3SW_EC	

Type text here



ROM Structure	NOTE
RDTR	For RDTR and debug port
LPFCW	For LPC and debug port
PCW0	
TPM0	Trusted Platform Module(TPM)
SD0	
CM0	CODE ROM
ENC_ROM	ENC Reserves
ME0	ME Connector
RF0	For RF function
ENCW	For BMI Function
RF_SD0	reserves RF component
NR0AD08	
DAS000	
SD00	
Sub00	
HostSub0	
U2_SD00	
Non_U2_SD00	



M.2 SSD1

LAN

WLAN

Media Card Reader

WWAN

58 PCIE0_L0_RXP
58 PCIE0_L0_RXN
58 PCIE1_L1_RXP
58 PCIE1_L1_RXN
57 PCIE2_L2_RXP
57 PCIE2_L2_RXN
57 PCIE3_L3_RXP
57 PCIE3_L3_RXN

73 PCIE4_RXP
73 PCIE4_RXN
66 PCIE5_RXP
66 PCIE5_RXN
76 PCIE6_RXP
76 PCIE6_RXN
67 PCIE7_RXP
67 PCIE7_RXN

PCIE0_L0_RXP
PCIE0_L0_RXN
PCIE1_L1_RXP
PCIE1_L1_RXN
PCIE2_L2_RXP
PCIE2_L2_RXN
PCIE3_L3_RXP
PCIE3_L3_RXN

PCIE4_RXP
PCIE4_RXN
PCIE5_RXP
PCIE5_RXN
PCIE6_RXP
PCIE6_RXN
PCIE7_RXP
PCIE7_RXN

UC1A
X G13
X F13
X J14
X H14
X G15
X F15
X J15
X K15
X H16
X J16
X F18
X G18
X J18
X K18
X H19
X G19

G11 P_GPP_RXP0
F11 P_GPP_RXN0
J10 P_GPP_RXP1
H10 P_GPP_RXN1
G8 P_GPP_RXP2/SATA0_RXP
F8 P_GPP_RXN2/SATA0_RXN
G6 P_GPP_RXP3/SATA1_RXP
F7 P_GPP_RXN3/SATA1_RXN

M9 P_GPP_RXP4
M8 P_GPP_RXN4
L7 P_GPP_RXP5
L6 P_GPP_RXN5
K7 P_GPP_RXP6
K8 P_GPP_RXN6
H6 P_GPP_RXP7
H7 P_GPP_RXN7

X L8 P_GPP_RXP8/SATA2_RXP
X L10 P_GPP_RXN8/SATA2_RXN
X K11 P_GPP_RXP9/SATA3_RXP
X J11 P_GPP_RXN9/SATA3_RXN
X J12 P_GPP_RXP10
X H12 P_GPP_RXN10
X J13 P_GPP_RXP11
X H13 P_GPP_RXN11

FP8
CPU@

PP16 REV0.92
PART 2/13

P_GFX_TXP0
P_GFX_TXN0
P_GFX_TXP1
P_GFX_TXN1
P_GFX_TXP2
P_GFX_TXN2
P_GFX_TXP3
P_GFX_TXN3
P_GFX_TXP4
P_GFX_TXN4
P_GFX_TXP5
P_GFX_TXN5
P_GFX_TXP6
P_GFX_TXN6
P_GFX_TXP7
P_GFX_TXN7

L3 P_GPP_TXP0
L1 P_GPP_TXN0
L4 P_GPP_TXP1
L2 P_GPP_TXN1
M4 P_GPP_TXP2/SATA0_TXP
M2 P_GPP_TXN2/SATA0_TXN
N3 P_GPP_TXP3/SATA1_TXP
N1 P_GPP_TXN3/SATA1_TXN

T2 P_GPP_TXP4
T4 P_GPP_TXN4
R1 P_GPP_TXP5
R3 P_GPP_TXN5
P2 P_GPP_TXP6
P4 P_GPP_TXN6
N2 P_GPP_TXP7
N4 P_GPP_TXN7

K2 P_GPP_TXP8/SATA2_TXP
K4 P_GPP_TXN8/SATA2_TXN
J4 P_GPP_TXP9/SATA3_TXP
J2 P_GPP_TXN9/SATA3_TXN
H3 P_GPP_TXP10
H1 P_GPP_TXN10
H4 P_GPP_TXP11
H2 P_GPP_TXN11

F4
F2
F3
E4
E1
C1
D5
E6
C6
D6
B6
C7
D8
B8
C8
A8

PCIE0_L0_TXP
PCIE0_L0_TXN
PCIE1_L1_TXP
PCIE1_L1_TXN
PCIE2_L2_TXP
PCIE2_L2_TXN
PCIE3_L3_TXP
PCIE3_L3_TXN

PCIE4_TXP
PCIE4_TXN
PCIE5_TXP
PCIE5_TXN
PCIE6_TXP
PCIE6_TXN
PCIE7_TXP
PCIE7_TXN

58 PCIE0_L0_TXP
58 PCIE0_L0_TXN
58 PCIE1_L1_TXP
58 PCIE1_L1_TXN
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57 PCIE2_L2_TXN
57 PCIE3_L3_TXP
57 PCIE3_L3_TXN

M.2 SSD1

LAN

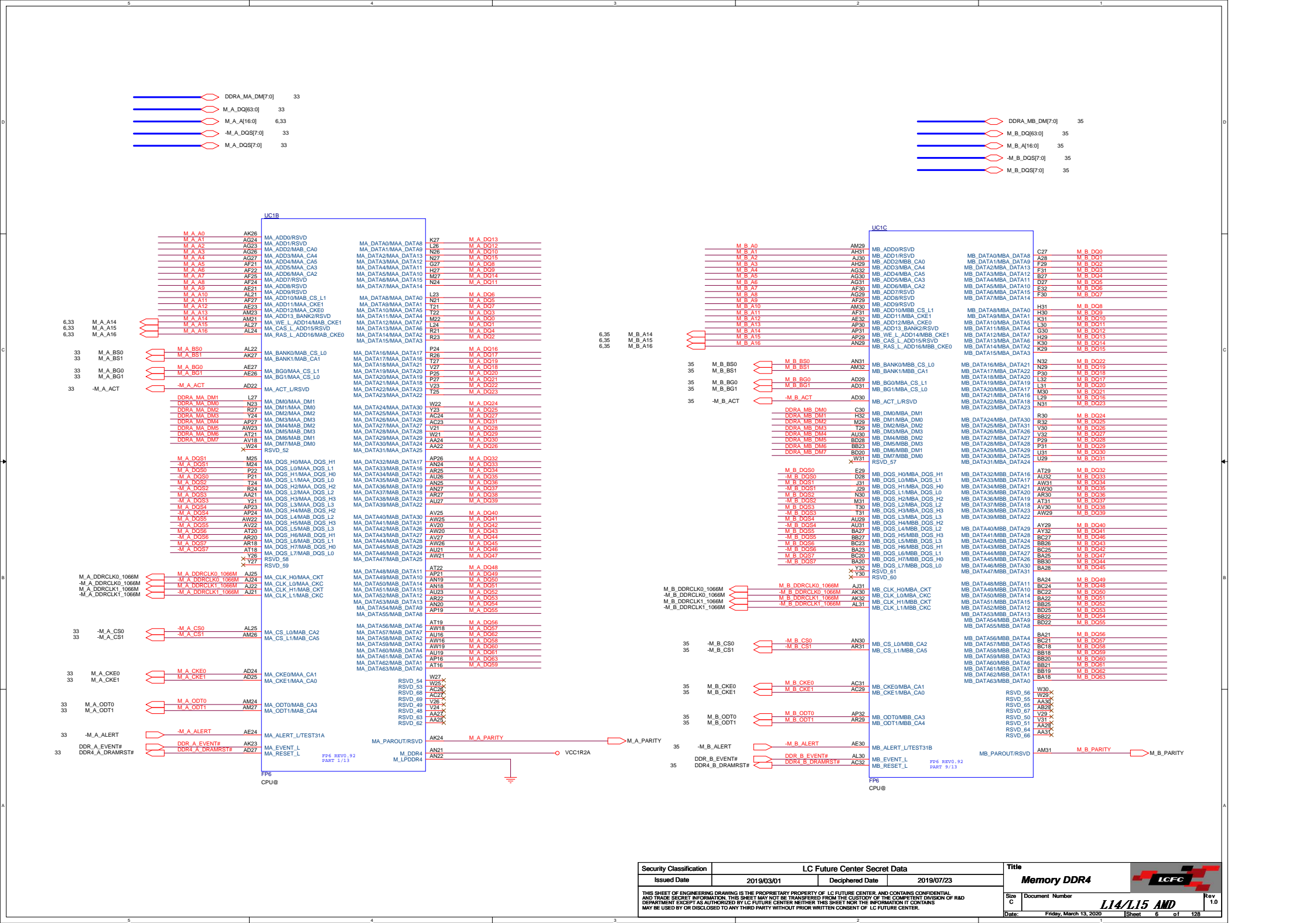
WLAN

Media Card Reader

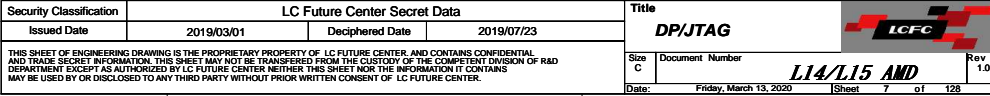
WWAN

PCIE4_TXP
PCIE4_TXN
PCIE5_TXP
PCIE5_TXN
PCIE6_TXP
PCIE6_TXN
PCIE7_TXP
PCIE7_TXN

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HDMI



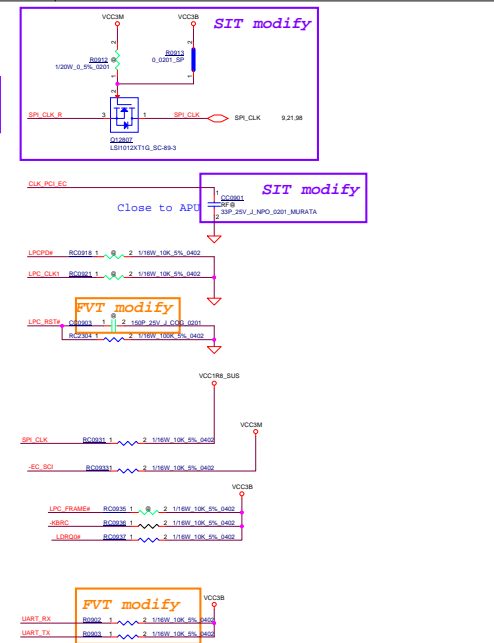
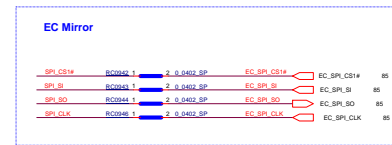
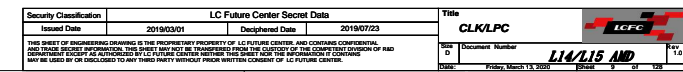
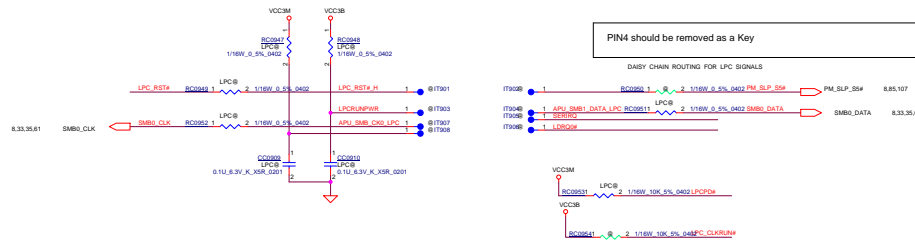
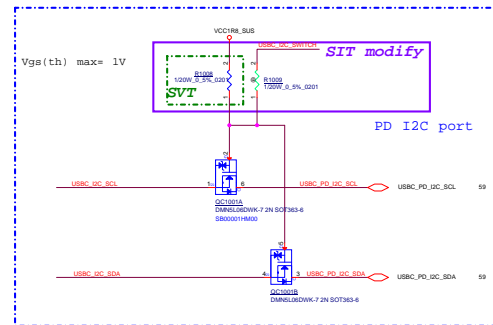
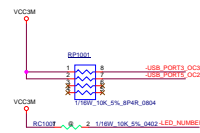
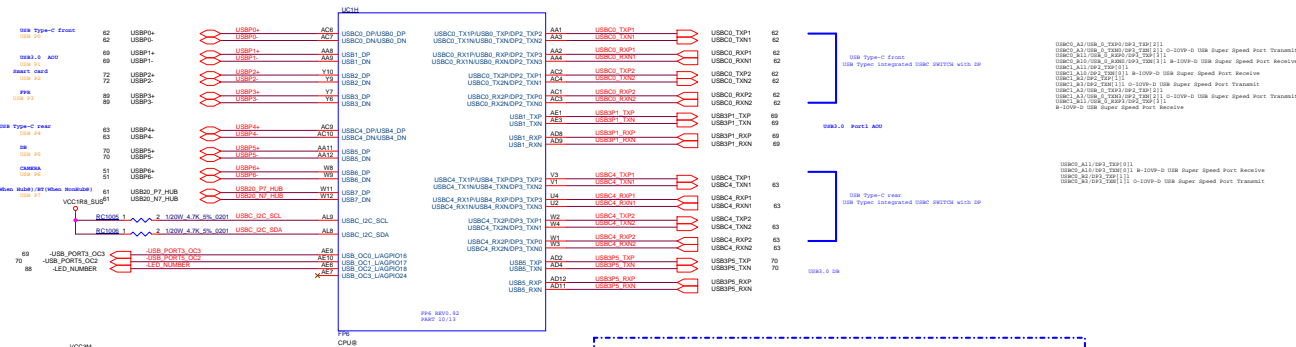



TABLE of Cystal (YC2)		
Vendor	LCFC P/N	Description
SEIKO	SJ10000IX00	S CRYSTAL 32.768KHZ 9PF X1A000141000200
SIWARD	SJ10000MU00	S CRYSTAL 32.768KHZ 9PF XTL721-L150-008

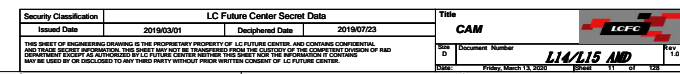


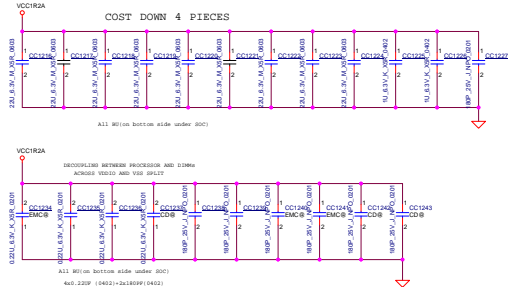
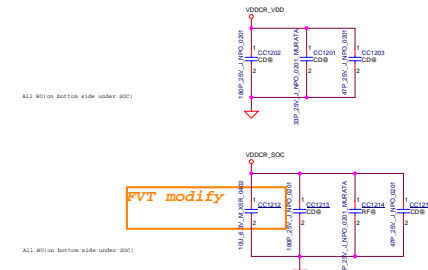
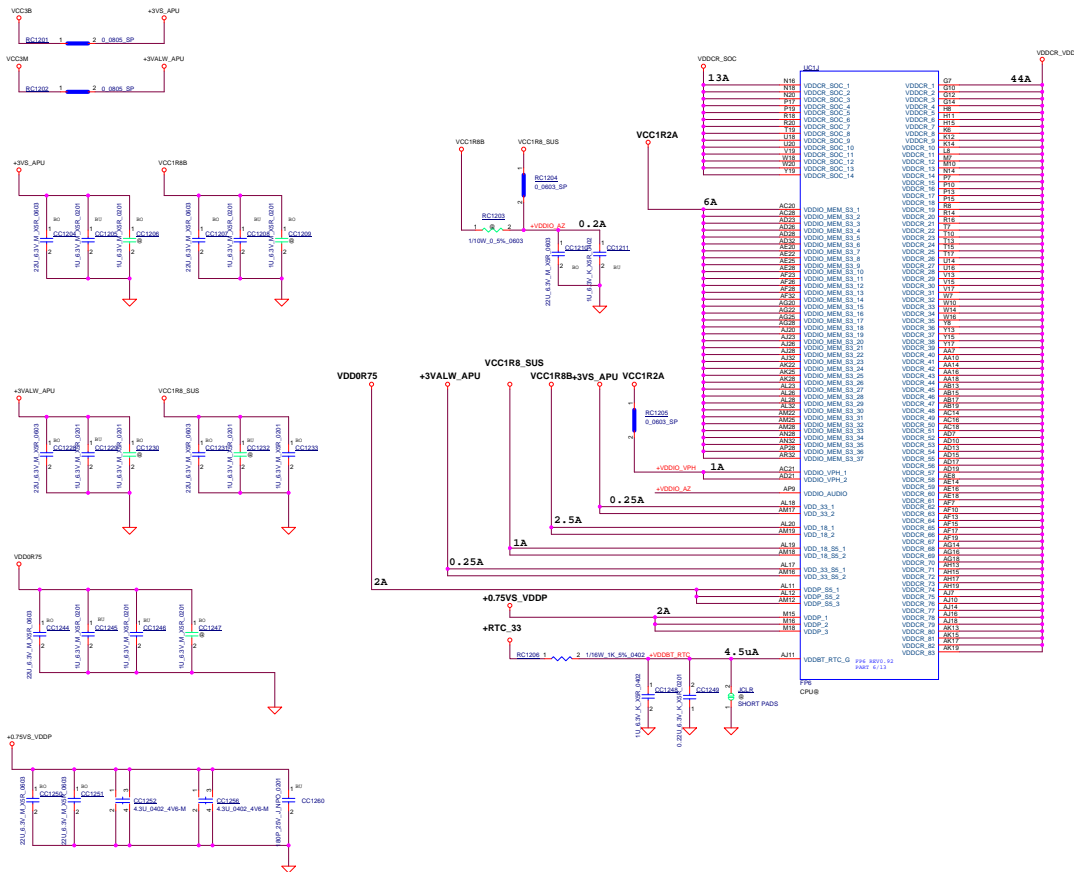
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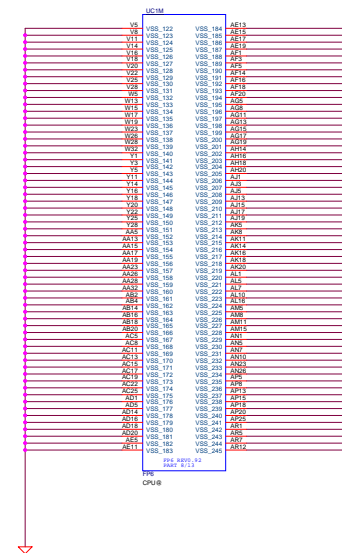


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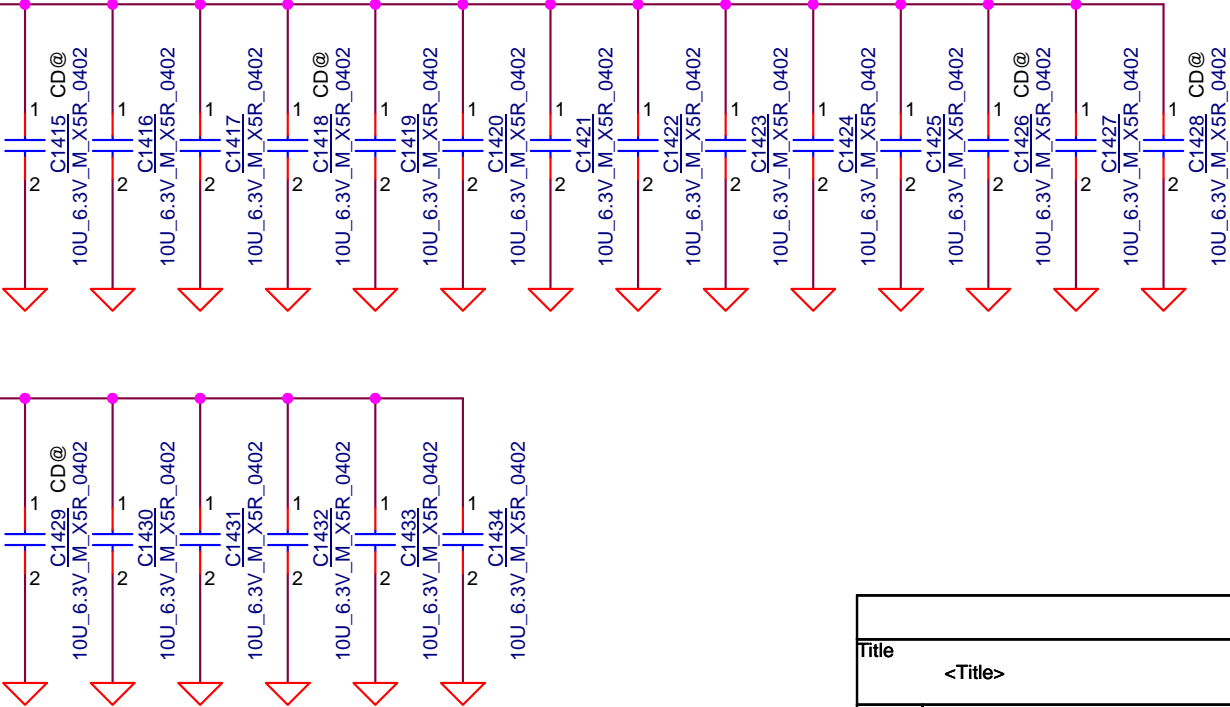
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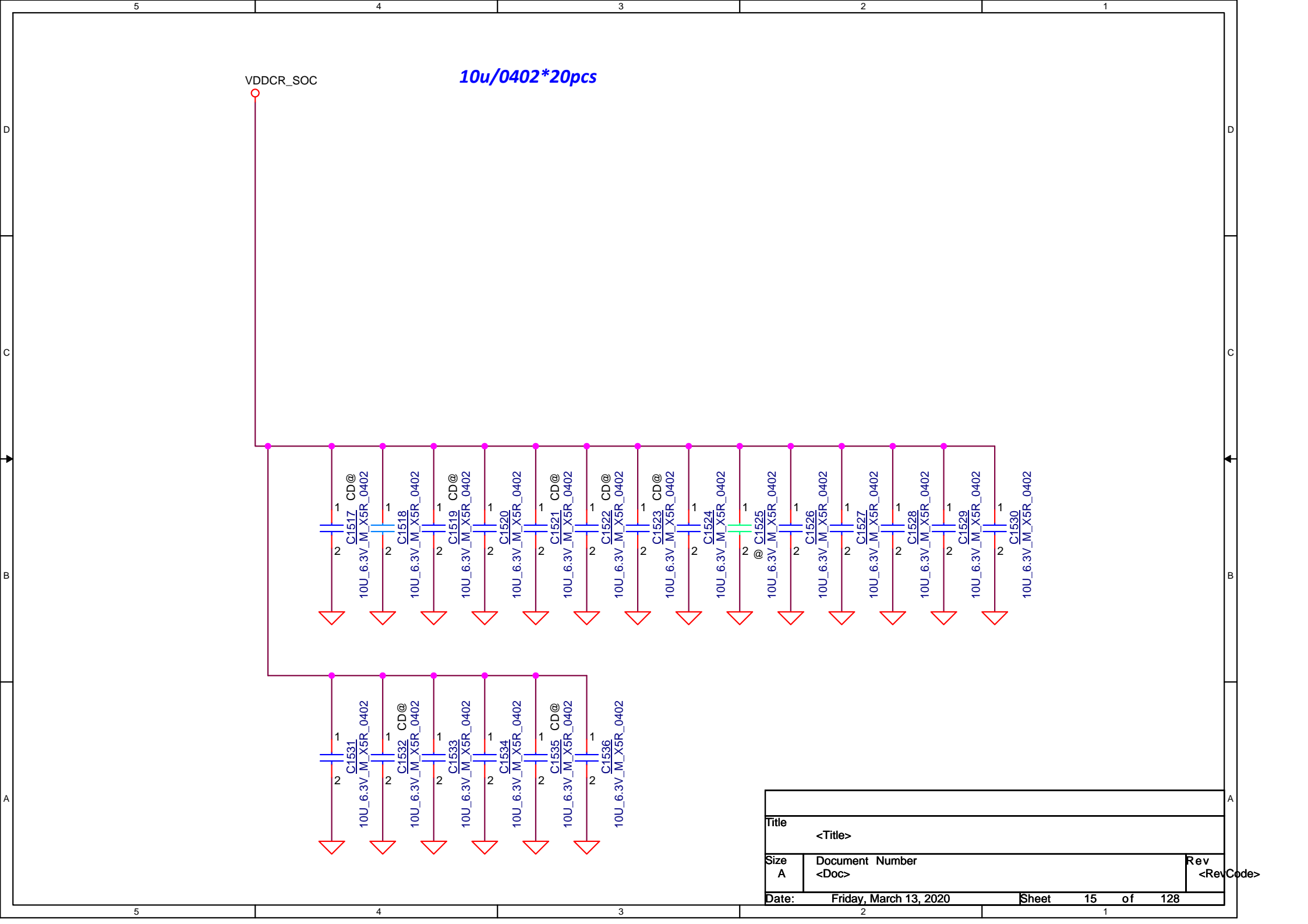
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VDDCR_VDD

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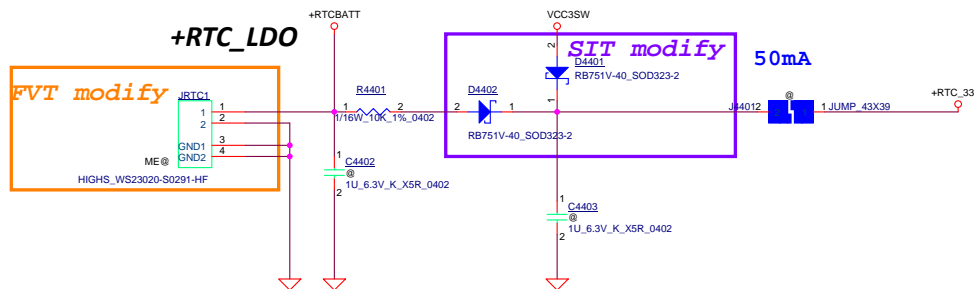
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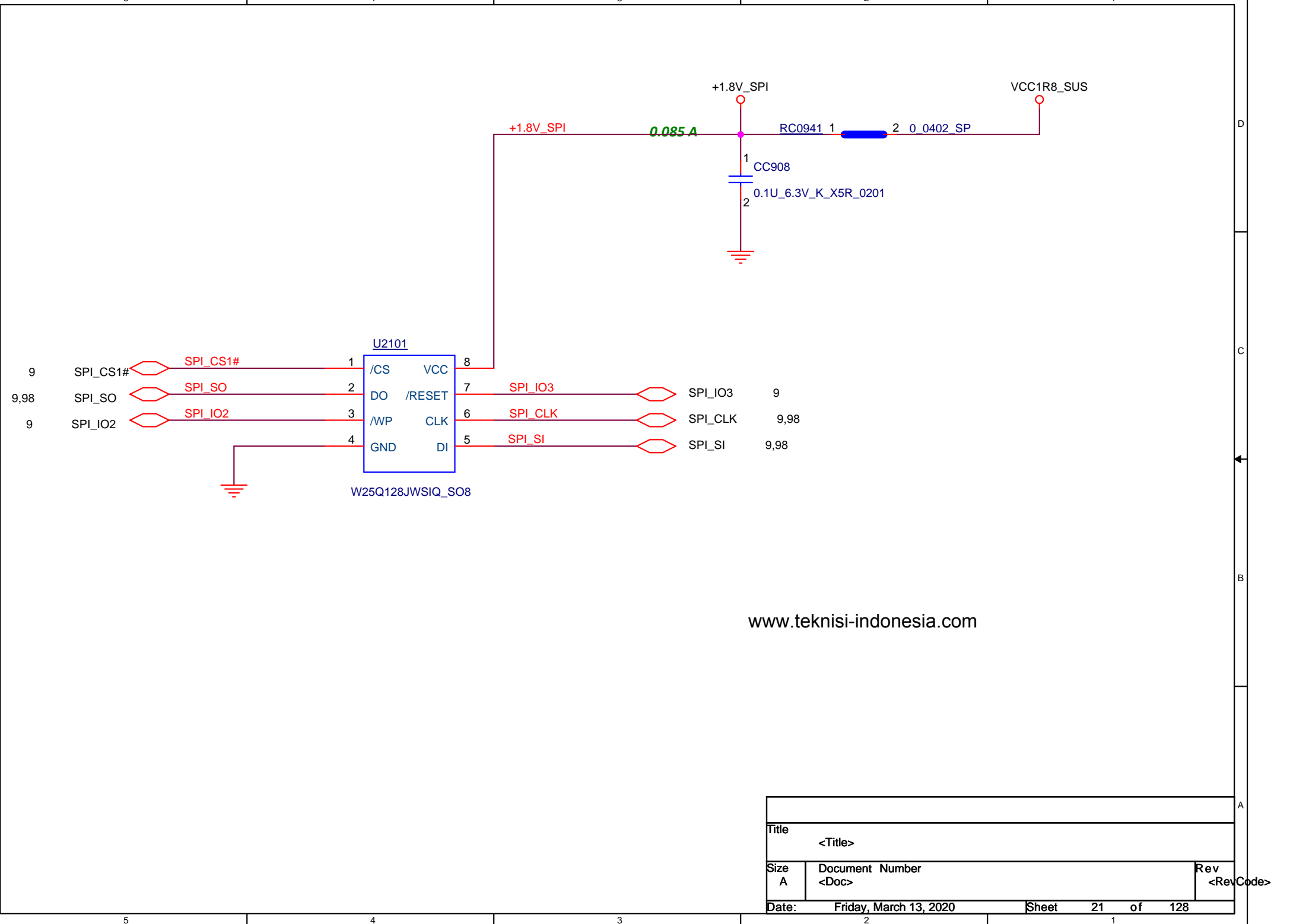
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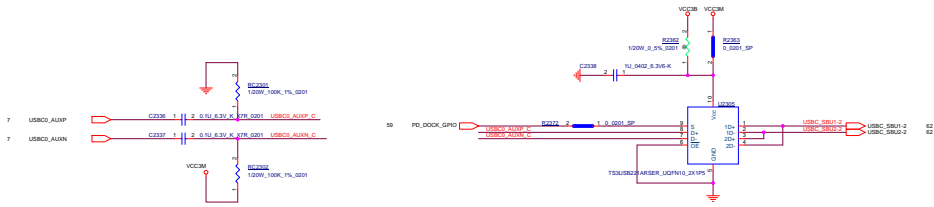
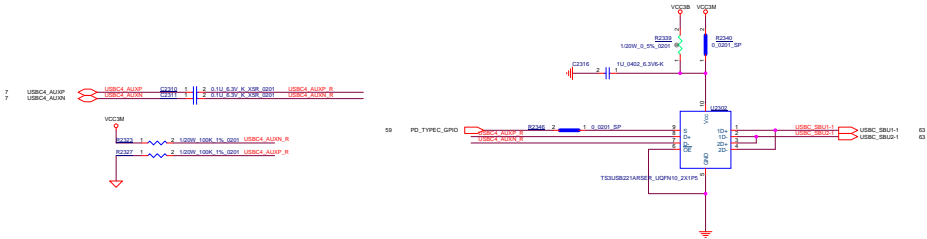
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Redriver IC



8.4 Device Functional Modes


Table 1. Truth Table

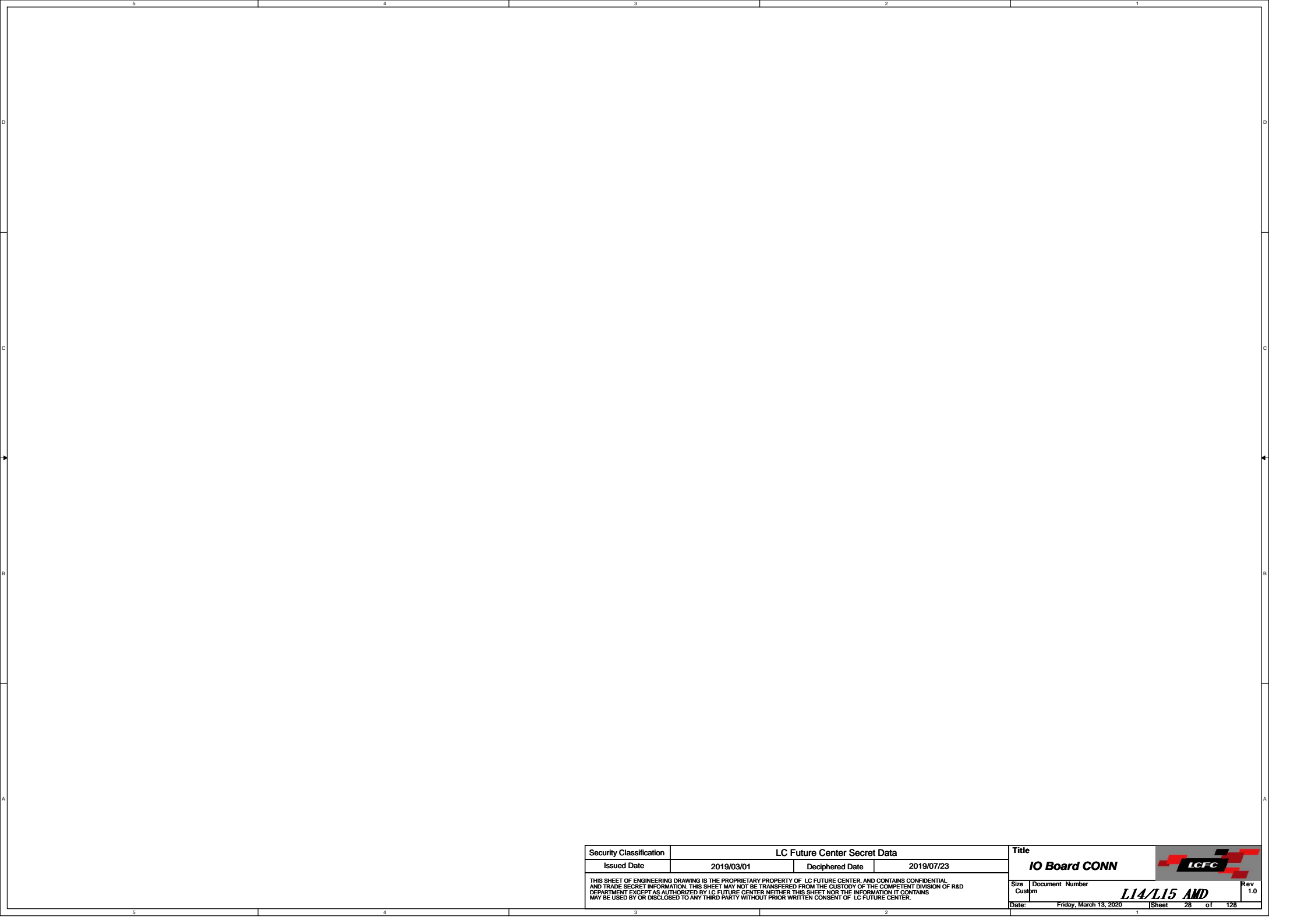
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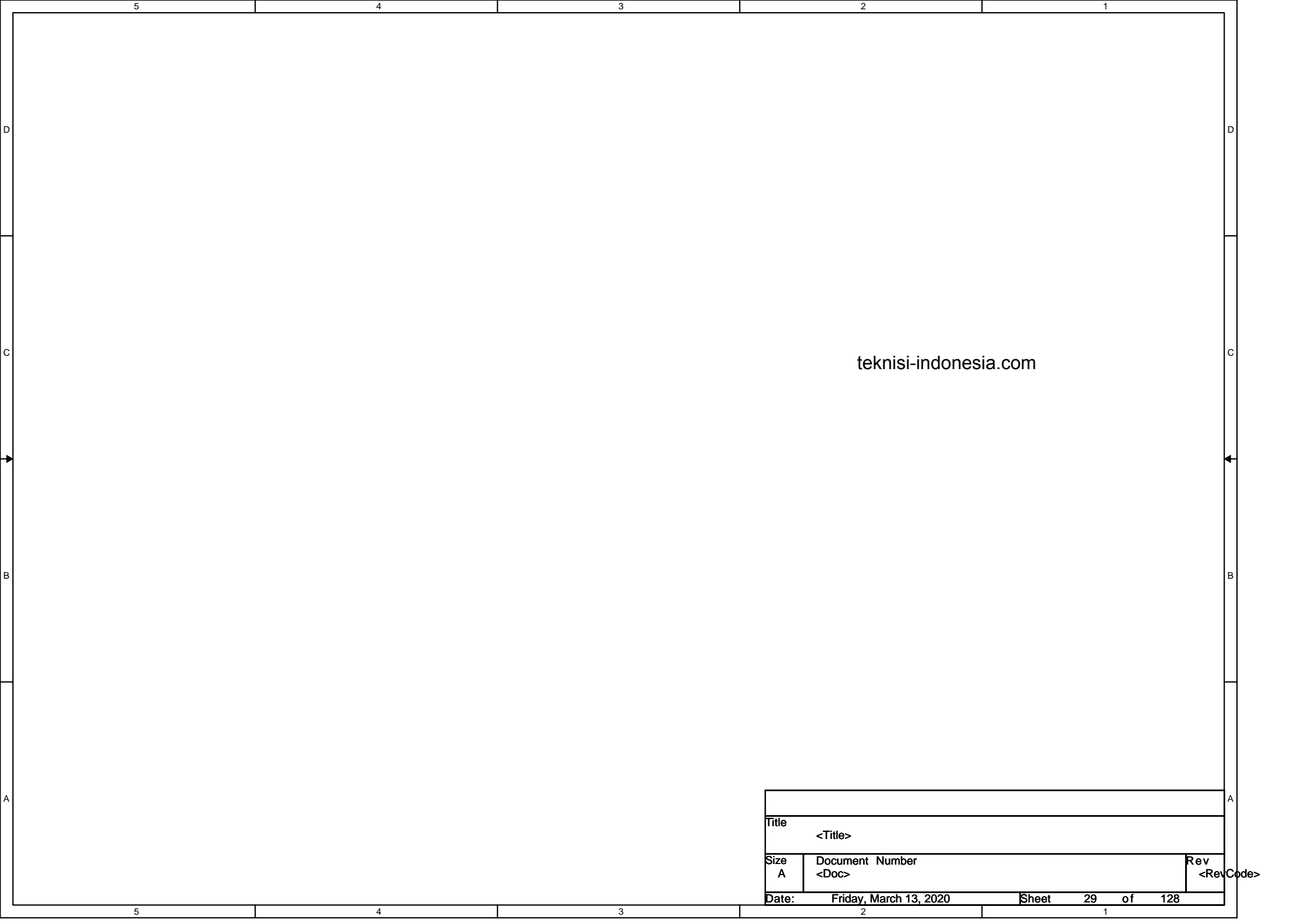
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			Type-C2 Redriver/CONN
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Issued Date					2019/03/01					Deciphered Date					2019/07/23										USB3.0 Redriver				
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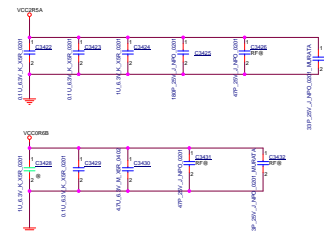
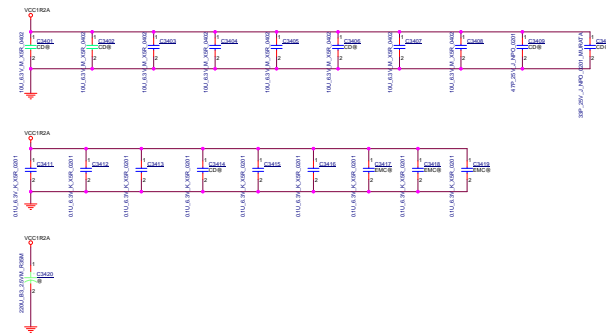
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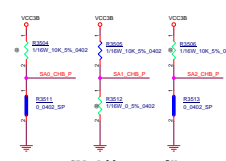
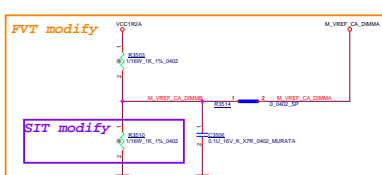
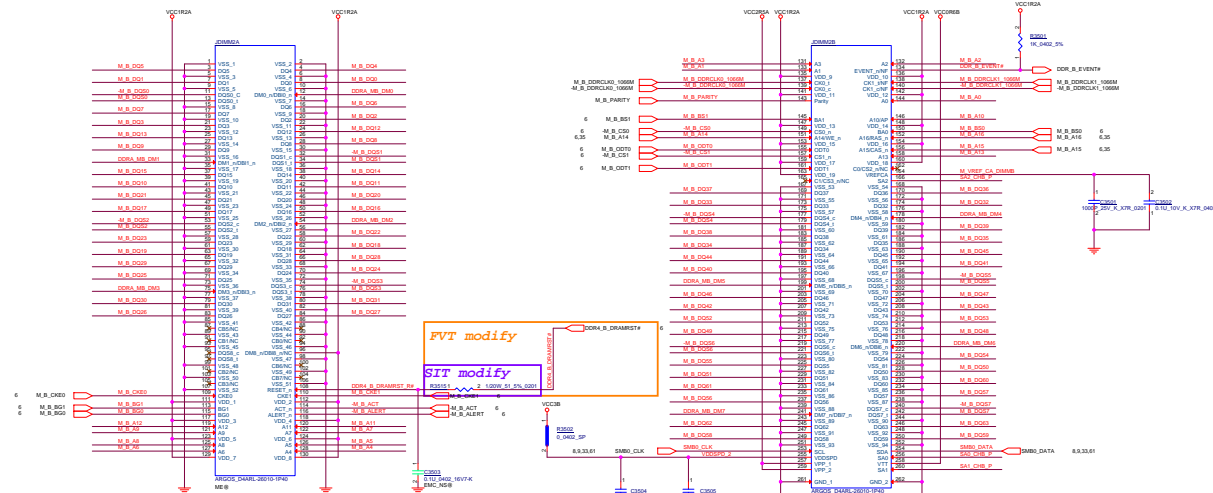
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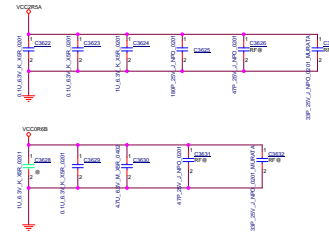
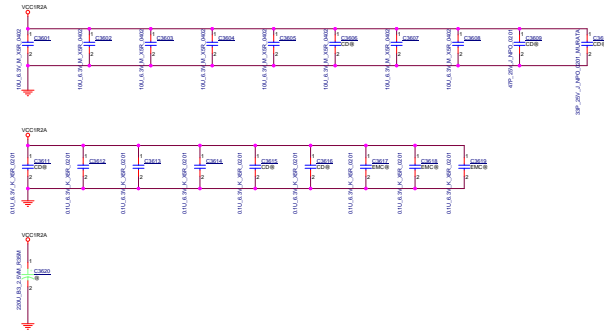




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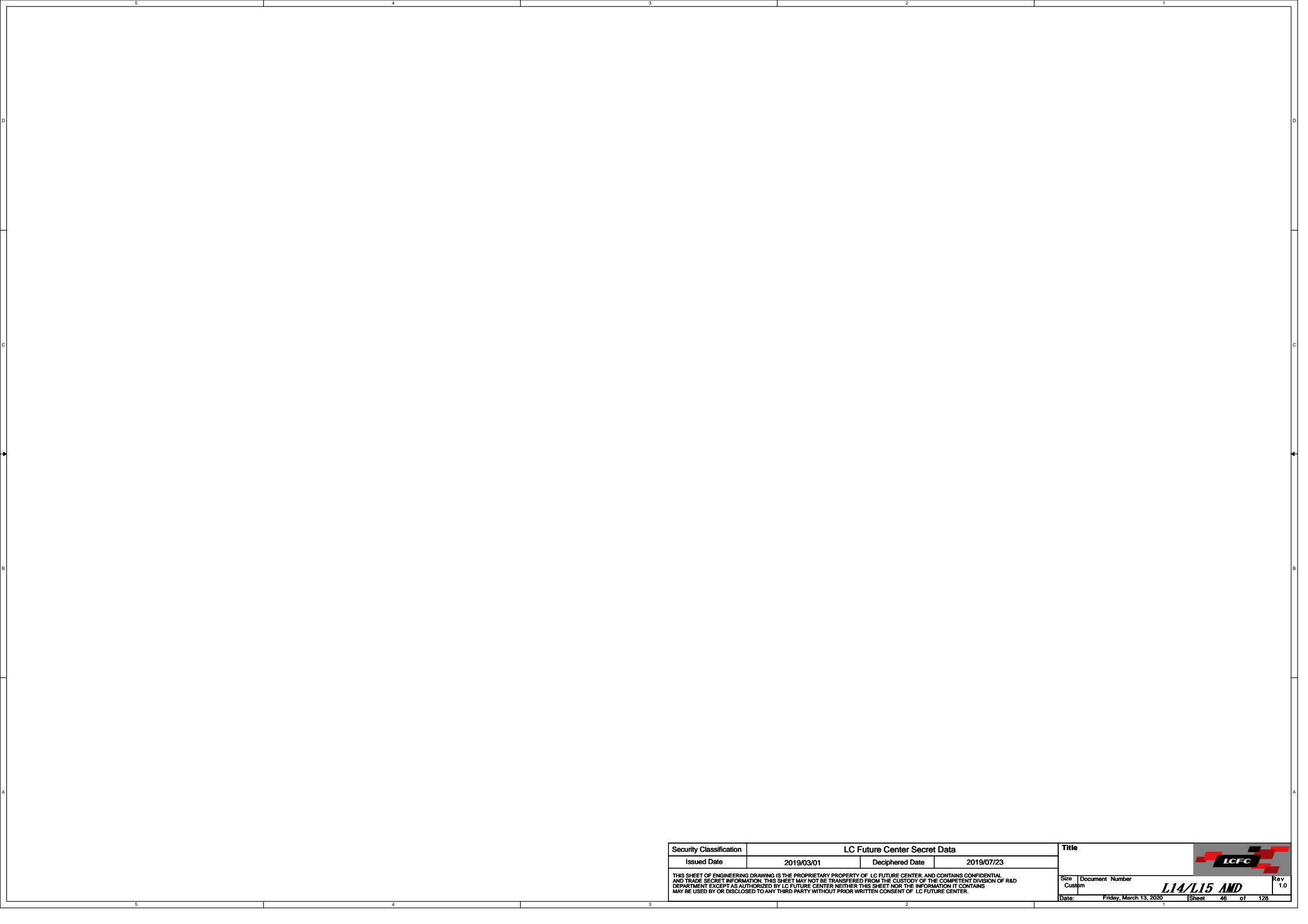
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Issued Date	2019/03/01	Decomposed Date	2019/07/23
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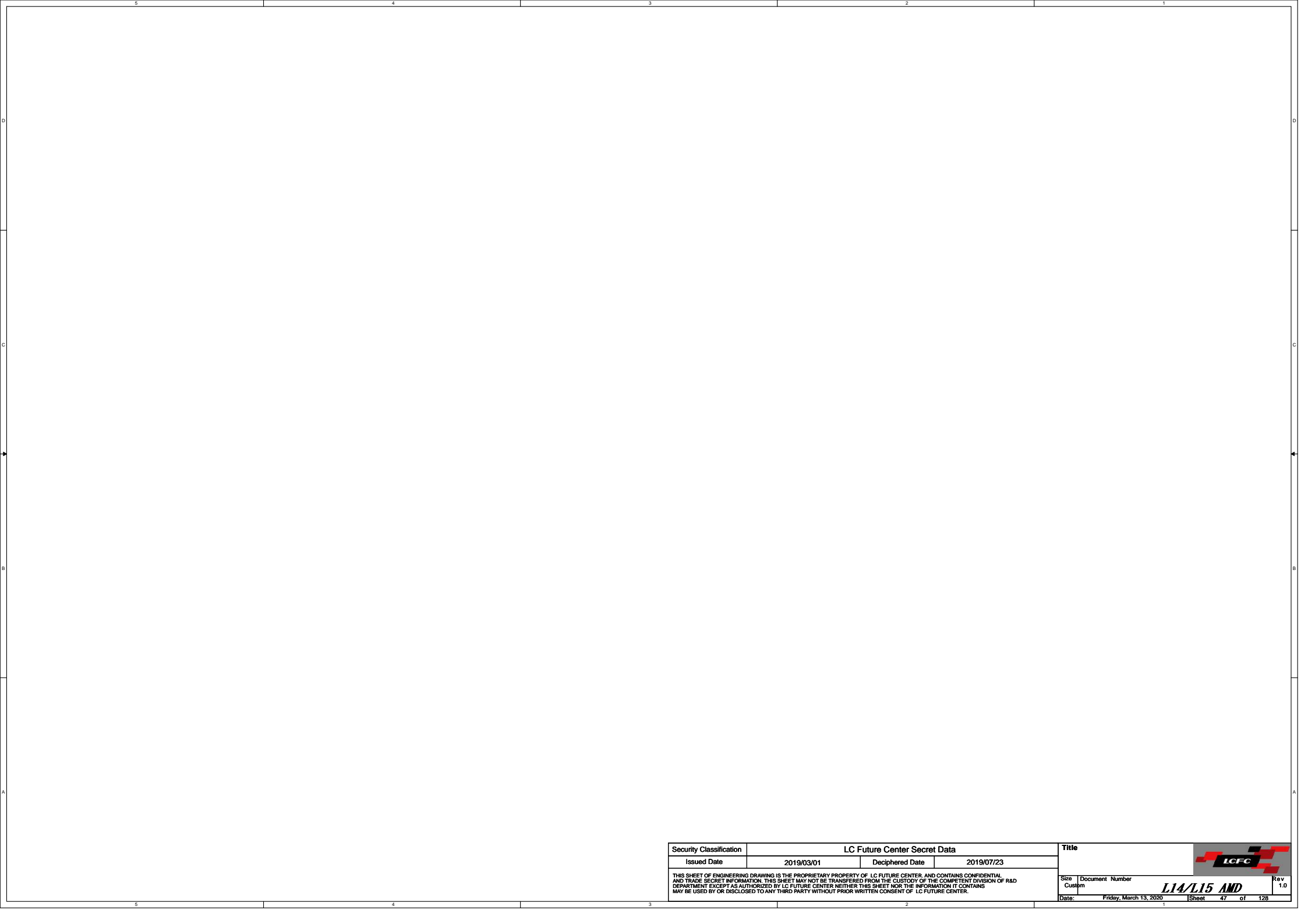



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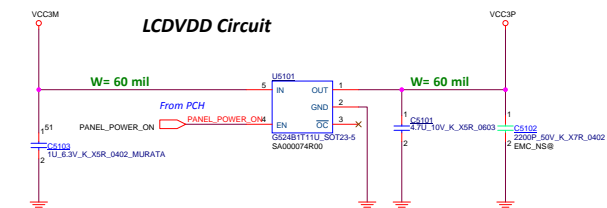
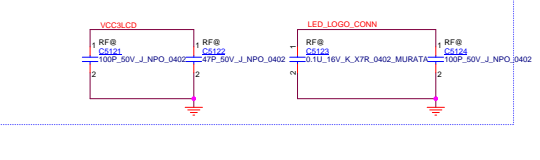
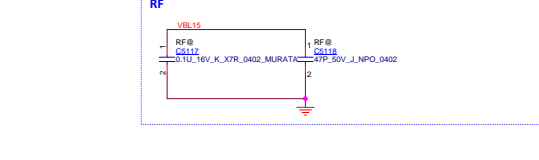
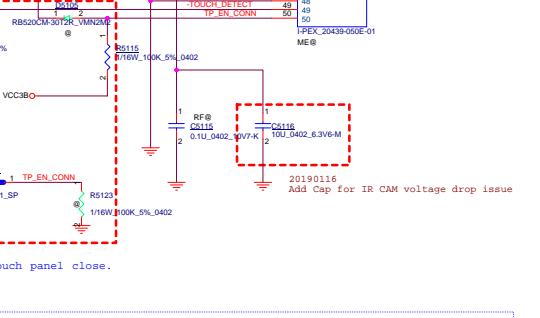
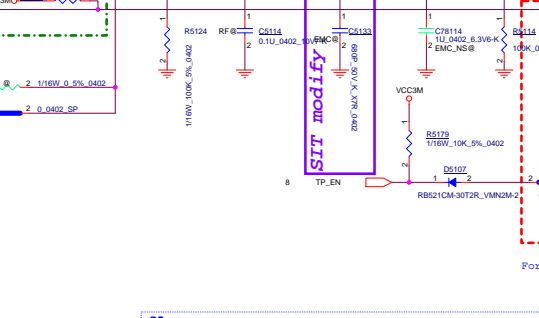
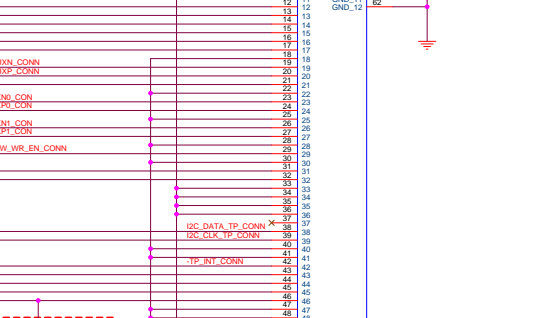
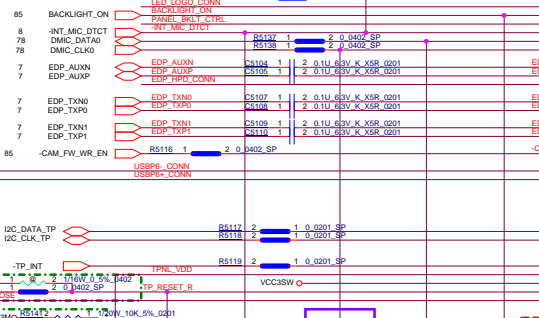
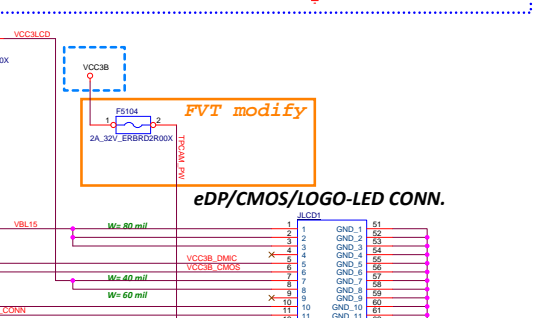
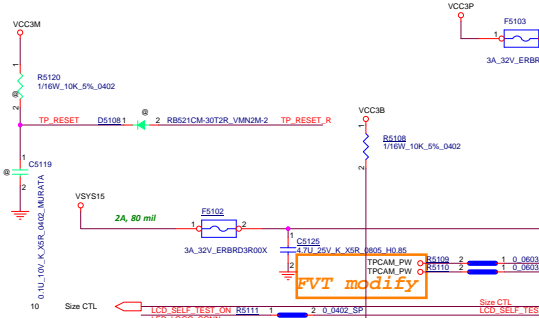
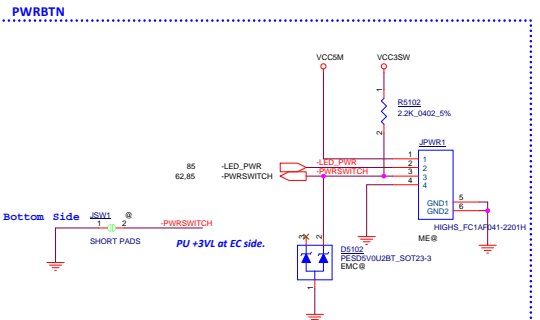
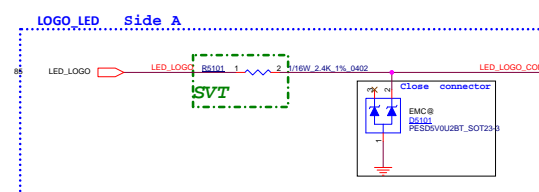
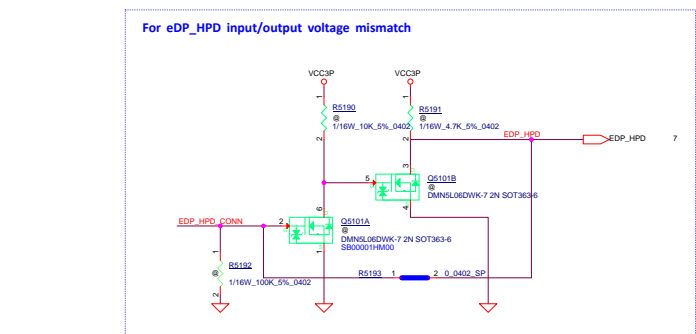
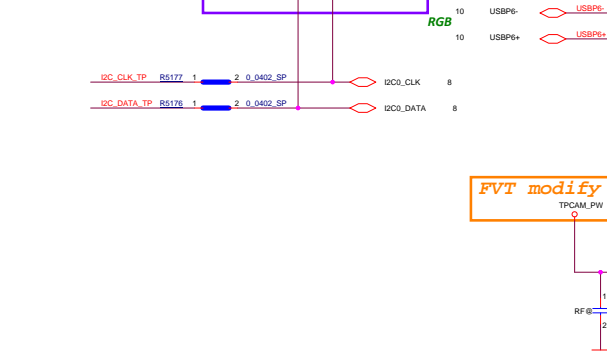
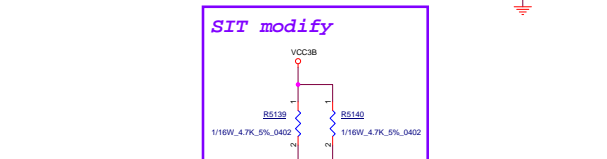
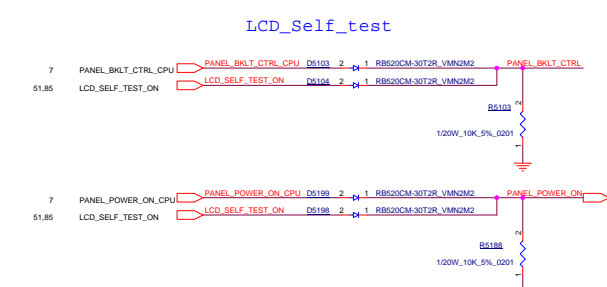



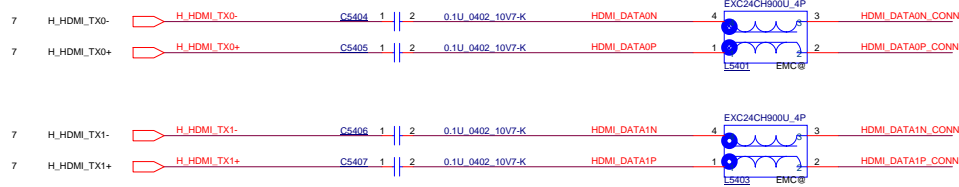
TABLE of POWER SWITCH (U5101)		
Vendor	LCFC P/N	Description
GMT	SA000074R00	S IC G524B1T11U SOT23 5P POWER SWITCH
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH

Status	Size CTL (EGPIO131)
15@ R5106	0 (GND Low)
14@ R5105	1 (NC High)

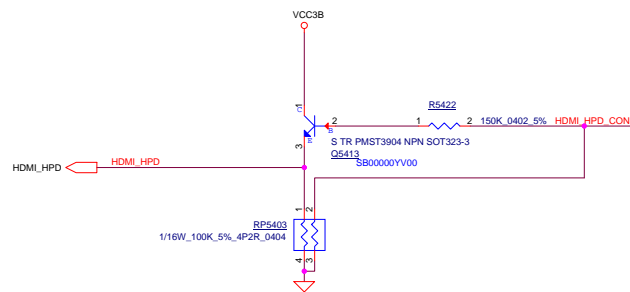
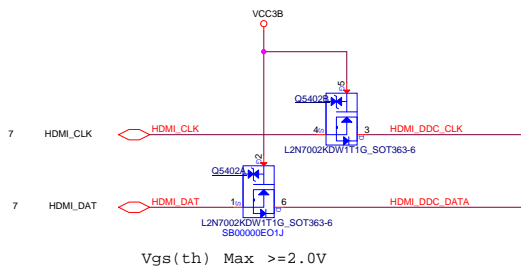
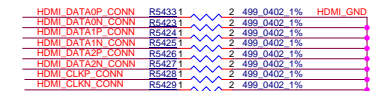
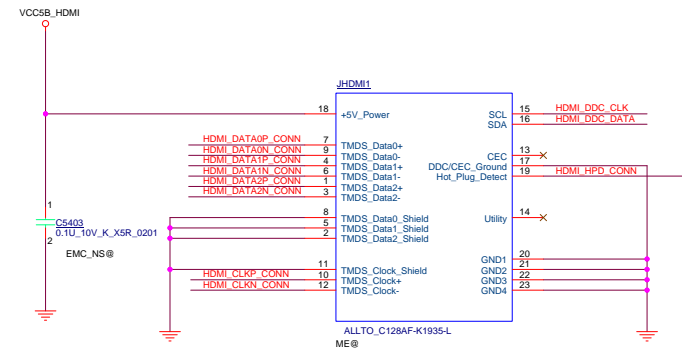
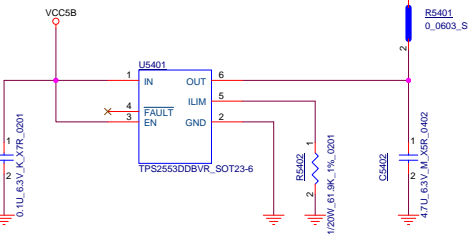
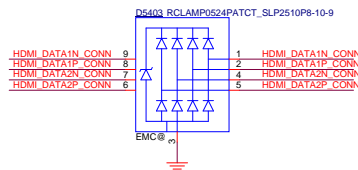
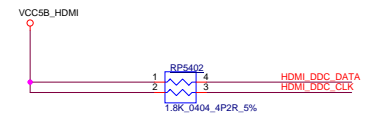
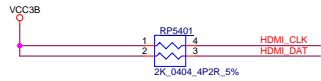
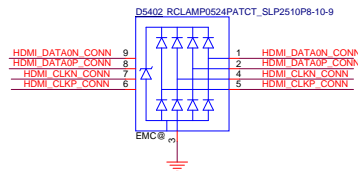
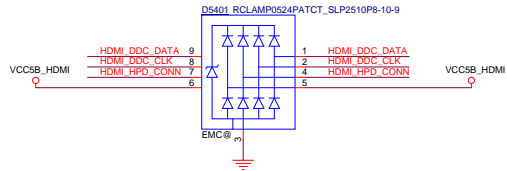


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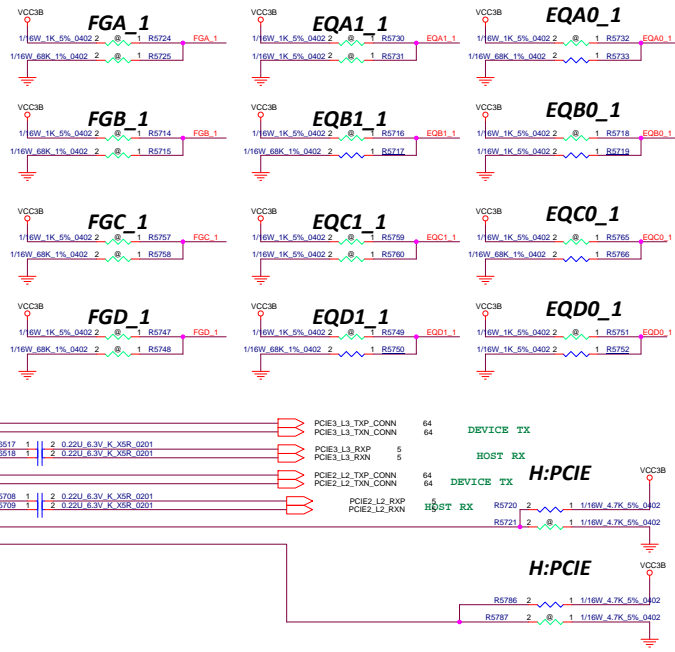
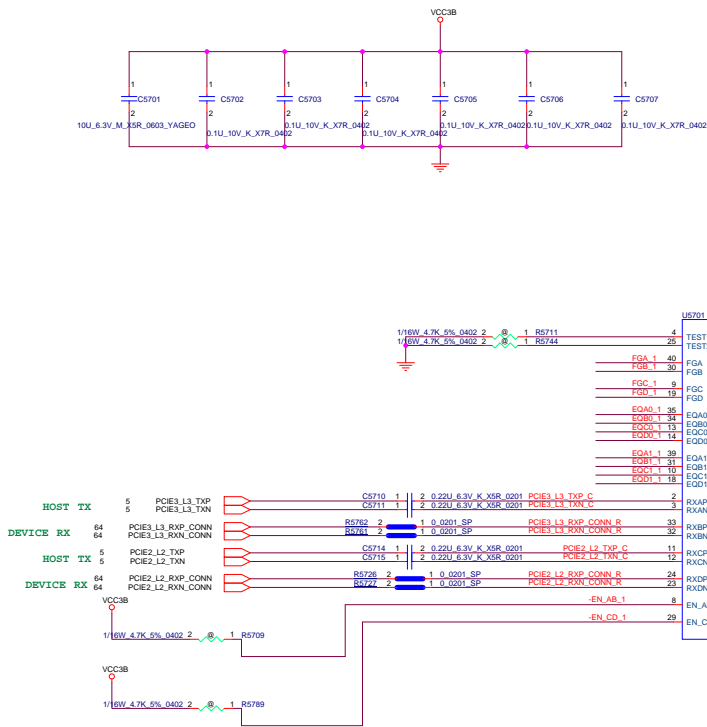
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Equalization Setting: EQA/B are the selection pins for the equalization selection

EQ		Equalizer setting (dB)			
A1/B1	A0/B0	@1.25GHz	@2.5GHz	@3GHz	@4GHz
0	0	0.4	1.8	2.4	3.9
0	R	0.6	2.3	3.2	4.9
0	F	0.8	2.9	3.9	5.8
0	1	1.0	3.5	4.6	6.6
R	0	2.1	4.4	5.3	7.2
R	R	2.3	4.9	5.9	7.9
R	F	2.5	5.3	6.4	8.5
R	1	2.7	5.8	7.0	9.1
F	0	3.7	6.5	7.7	9.7
F	R	3.9	6.9	8.1	10.2
F	F	4.1	7.3	8.5	10.6
F	1	4.3	7.6	8.9	11.0
1	0	5.4	8.4	9.5	11.4
1	R	5.6	8.7	9.8	11.8
1	F	5.8	9.0	10.2	12.1
1	1	5.9	9.2	10.4	12.5

Flat Gain Setting: FGA/B are the selection bits for the DC gain

Flat Gain Settings	
FGA/B	dB
0	-3.5
R	-1.5
F	0 (Default)
1	+1.5

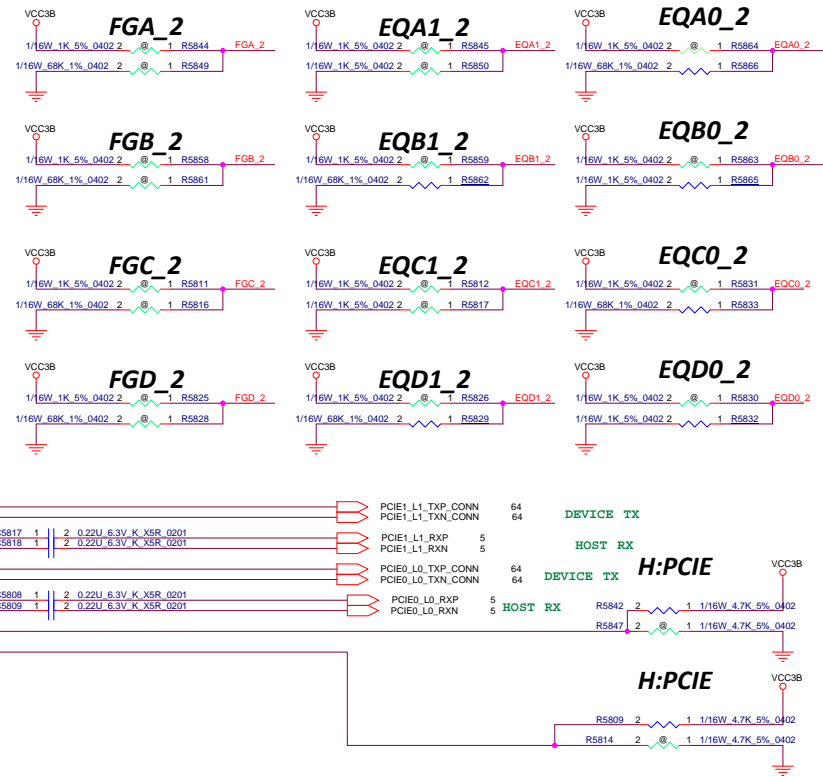
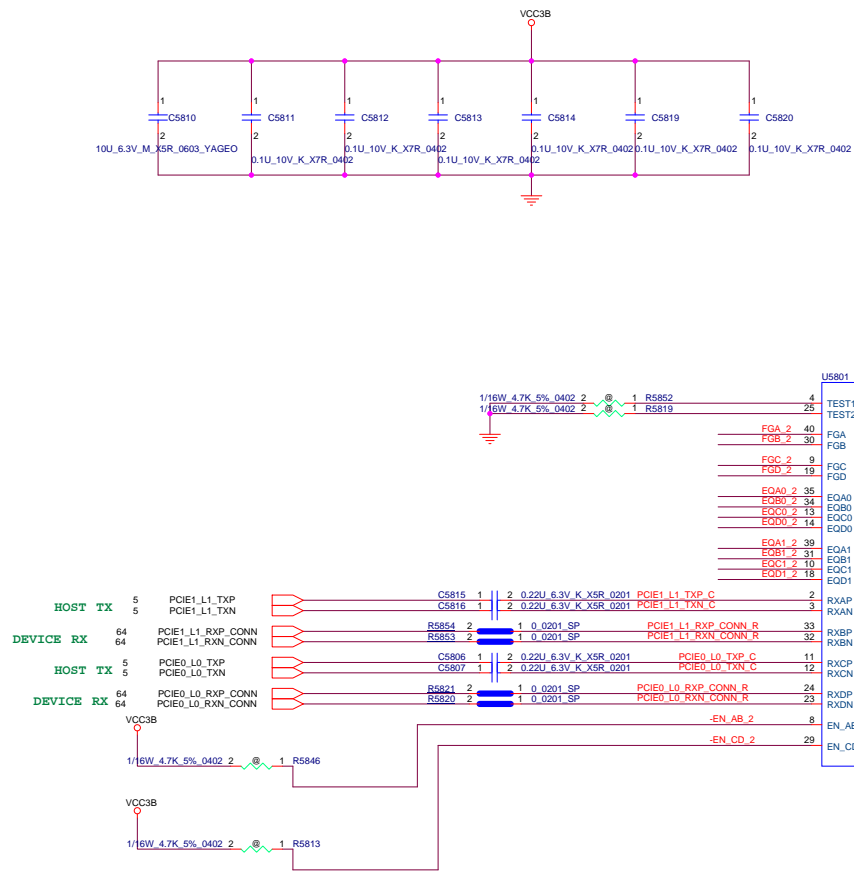
-1dB compression point output Swing Setting:

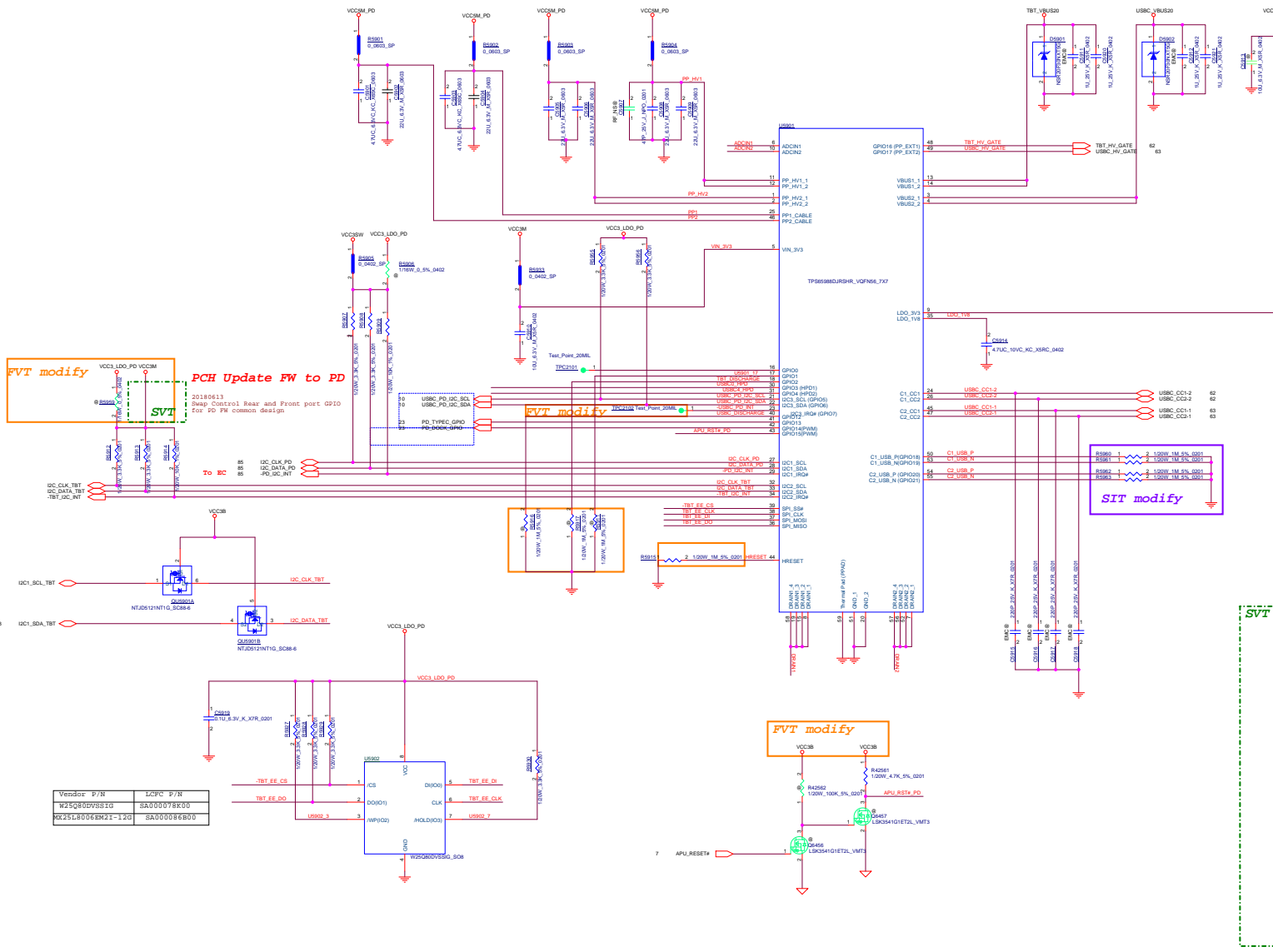
Output Linear Swing Settings	
SWA/B	mVppd
0	990
R	1050
F	1000 (Default)
1	1120

EL480/580 Setting					
TX EQ	TX SW	TX Gain	RX EQ	RX SW	RX Gain
A1:R	1	F	B1:0	1	F
A0:F			B0:1		
TX EQ	TX SW	TX Gain	RX EQ	RX SW	RX Gain
A1:R	1	F	B1:0	1	F
A0:F			B0:1		

For 12902A
0 means , pull down to GND thru 1K ohm
F , Floating
1 , pull up to VDD thru 1K ohm
R , pull down to GND thru 68K ohm.

Channel Enable Setting	
EN #	Setting
0	Enabled (Default)
1	Disabled





ADCIN1 BUS POWER CONFIGURATION

DIV MIN	DIV MAX	CONFIGURATION
0.00	0.18	BP_NoResponse
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

← LOGIC

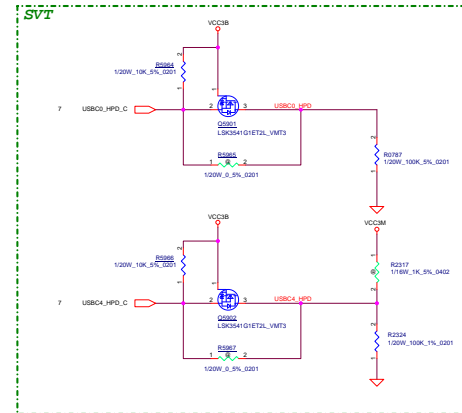
ADCIN2 I2C Address Setting

DIV MIN	DIV MAX	I2C Unique Address [3:1]	ADC_ADDR_DECODE_C1	ADC_ADDR_DECODE_C2
0.00	0.18	000b	100b	
0.20	0.38	001b	101b	
0.40	0.58	010b	110b	
0.60	1.00	011b	111b	

← LOGIC

I2C Address


I2C1 (to EC)	TBT PORT	0x46/0x47
USBC PORT	0x4E/0x4F	
TBT PORT	0x70/0x71	
I2C2 (to AR)	USBC PORT	0x7E/0x7F



Vendor P/N	LCFC P/N
W25Q64VSSIG	SA000078K00
W25L8064KZT-120	SA000086K00

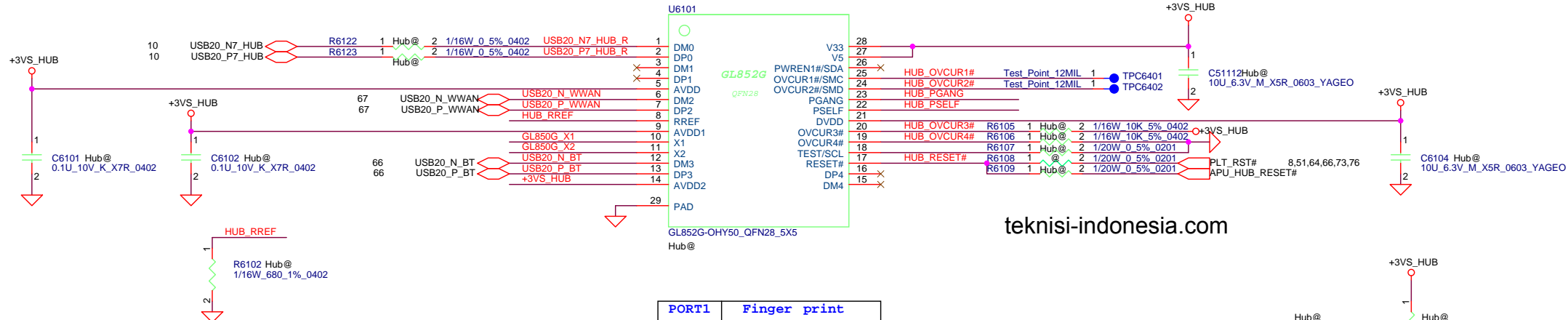
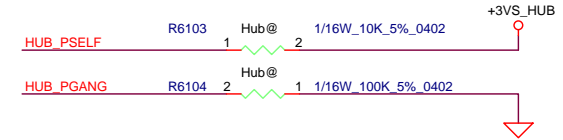
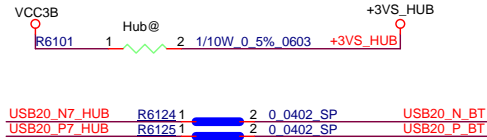
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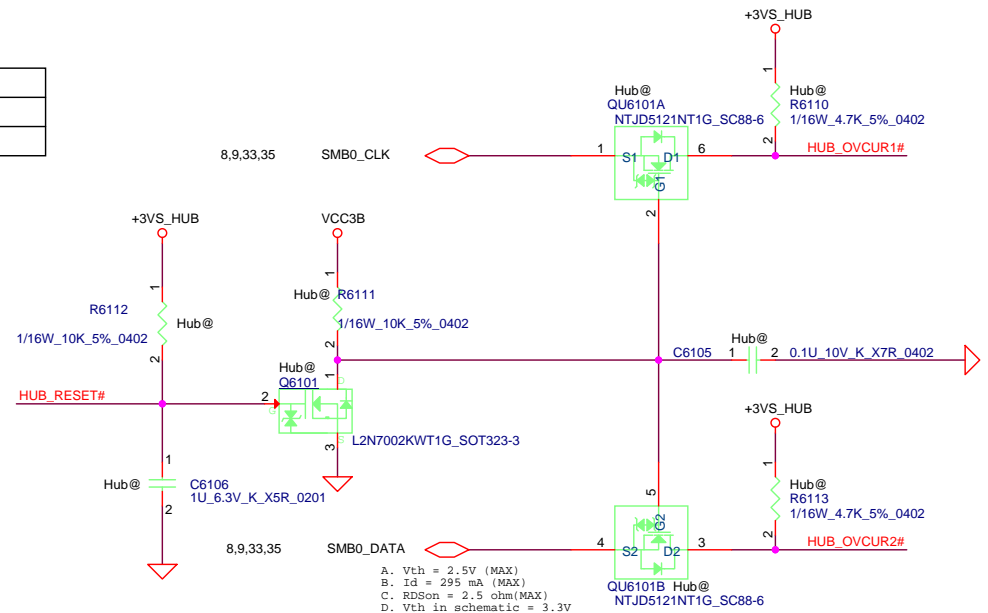
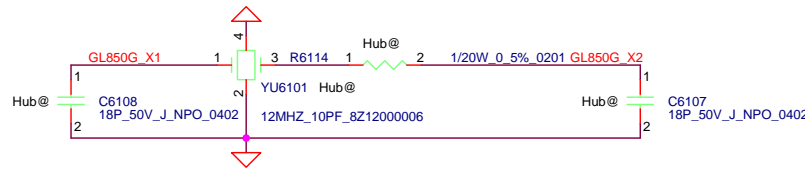
FVT modify

Adding NonHub@ and Hub@

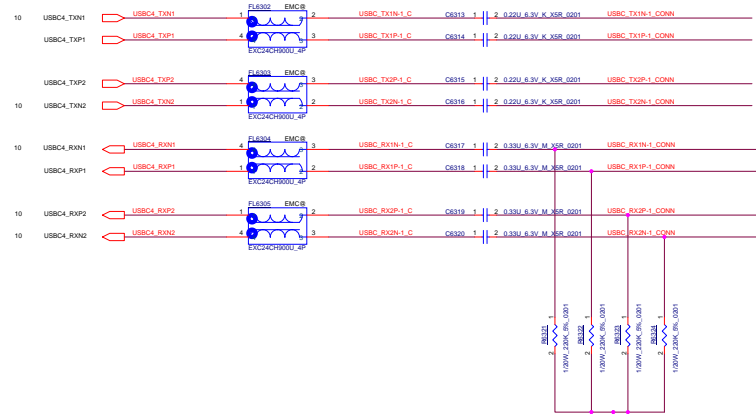
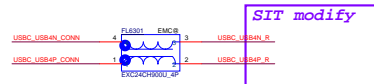
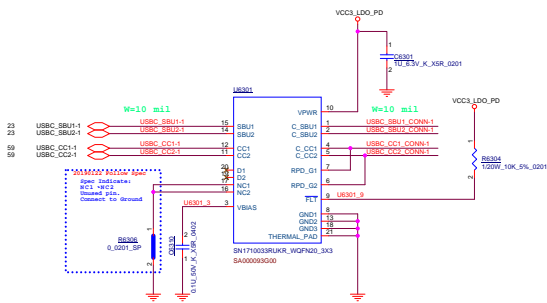


PORT1	Finger print
PORT2	WWAN
PORT3	BT

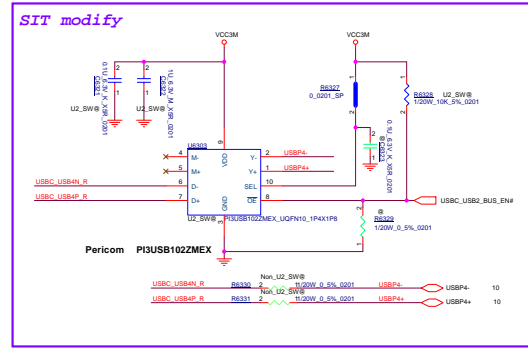
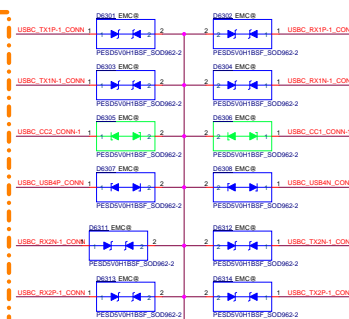
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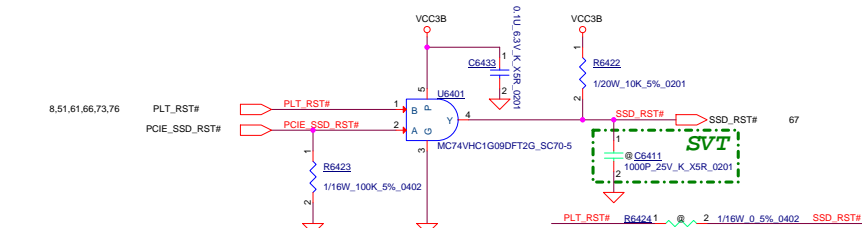



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				Sheet	61 of 128
				Rev	1.0




Co-Lay





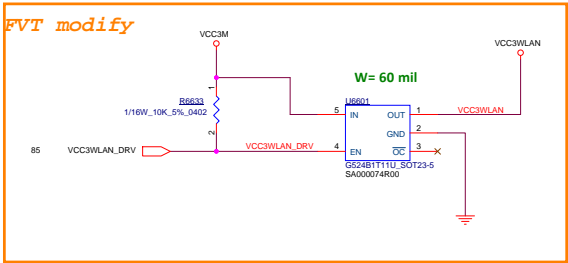
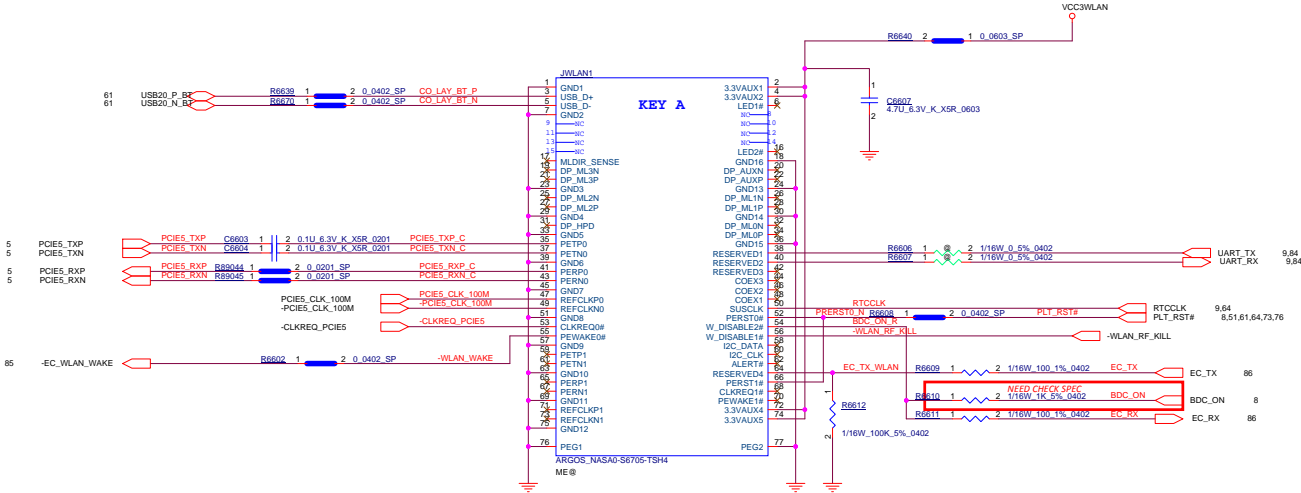
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Size		Document Number		Date		Rev
Custom		L14/L15 AMD		Friday, March 13, 2020		1.0
				Sheet		65 of 128

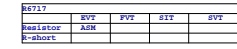
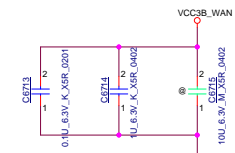
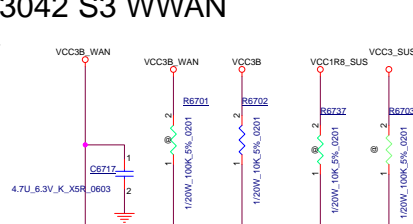
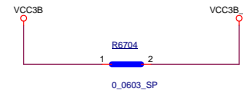
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VCC3B		VCC3B	7,8,9,12,23,33,35,51,54,57,58,59,61,64,67,70,73,76,78,85,88,89,91,92,98,101,106,127

TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR



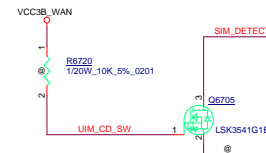
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H=2.00mm Connector




M.2 module side	Description	MIMO mode
L850-GL,L830-EB	#68=NC	2
L860-GL (#68= antenna cfg)	#68=internal pull up(100KΩ)	4


```
20181114
Add mos for SIM_DETECT function
```



State #	Module Configuration Decodes				Module Type and Main Host Interface	Port Configuration	Module
	CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)			
0	GND	GND	GND	GND	SSD - SATA	N/A	
1	GND	GND	GND	NC	SSD - PCIe	N/A	
2	GND	GND	NC	GND	WWAN - PCIe	0	
3	GND	GND	NC	NC	WWAN - PCIe	1	
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0	WWAN L850
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1	
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2	
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3	
8	NC	GND	GND	GND	WWAN - SSIC	0	WWAN L830
9	NC	GND	GND	NC	WWAN - SSIC	1	
10	NC	GND	NC	GND	WWAN - SSIC	2	
11	NC	GND	NC	NC	WWAN - SSIC	3	
12	NC	NC	GND	GND	WWAN - PCIe	2	
13	NC	NC	GND	NC	WWAN - PCIe	3	
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined	WWAN L860
15	NC	NC	NC	NC	No Module Present	N/A	

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				Sheet	67 of 128
				Rev	1.0

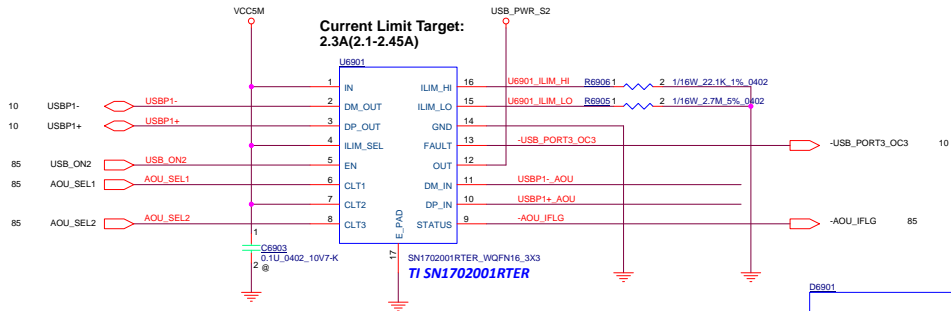
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L14/L15 AMD

USB AOU

VCC5M 51,70,84,85,103,106,107,108,109,110,127,128
USB_PWR_S2 USB_PWR_S2



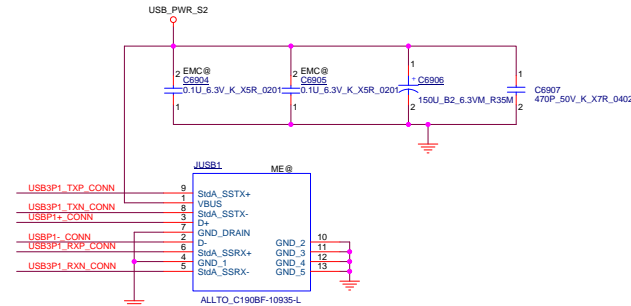
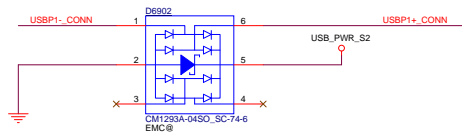
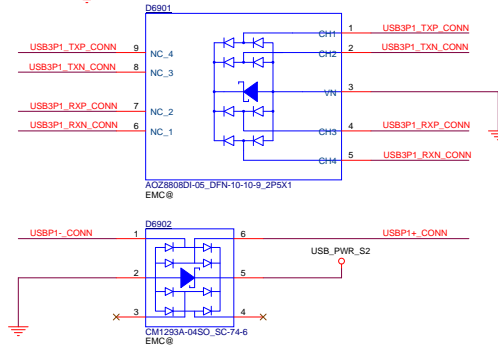
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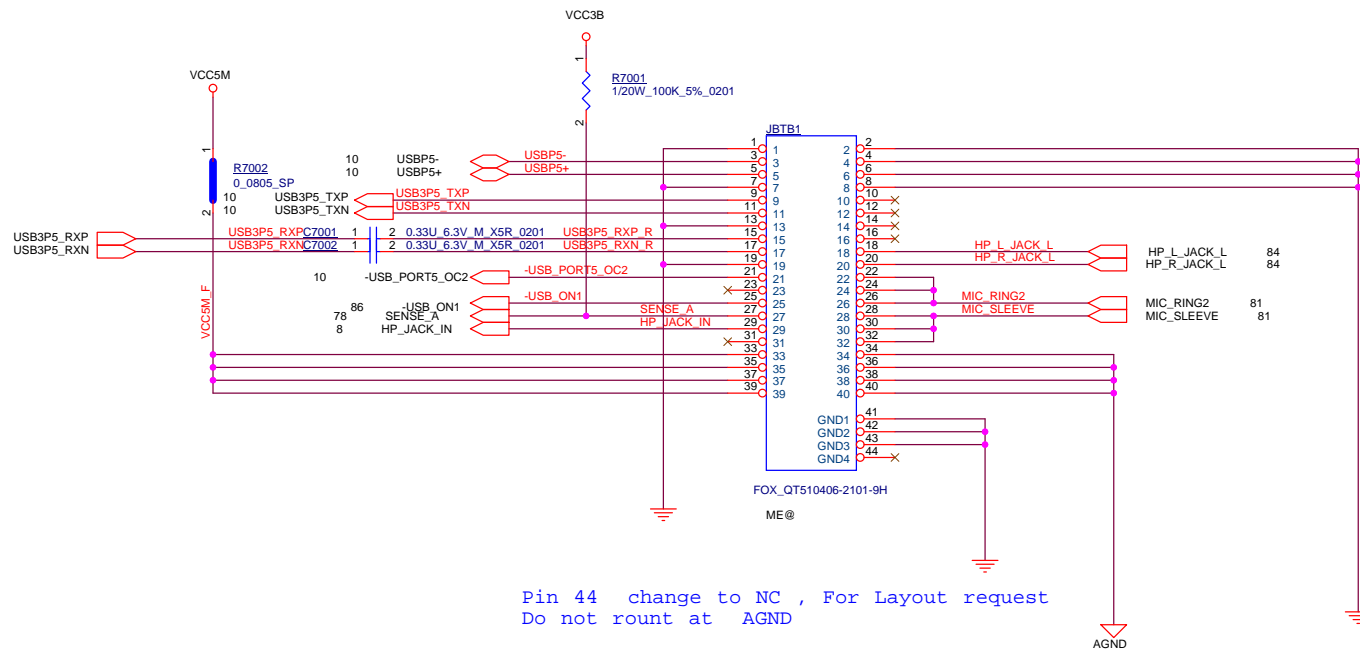



TABLE of POWER SWITCH (U6401)

Vendor	LCFC P/N	Description
T1	SA00008HF00	S IC SN1702001RTER WQFN 16P USB CHARGING
DIODES	SA00009D800	S IC PI5USB2546HZHEX TQFN 16P CONTROLLER


CLT1	CLT2	CLT3	ILIM_SEL	MOD
0	0	0	X	DCH OUT held low
1	1	1	1	CDP Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2 Data Connected
1	1	0	X	SDP1 Data Connected
0	1	0	X	SDP1 Data Connected
1	0	0	X	DCP_Short Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto Data Disconnected and Power Wake Function Active



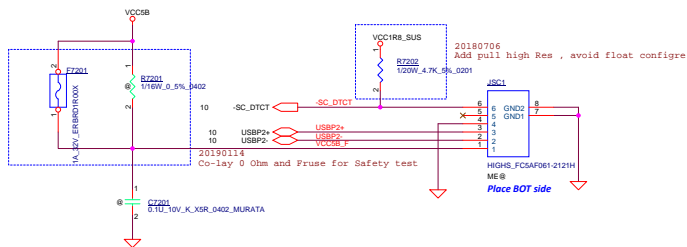


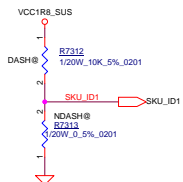
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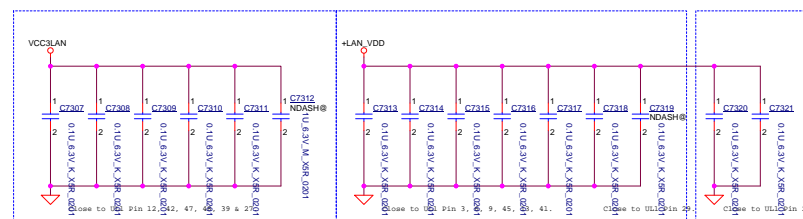
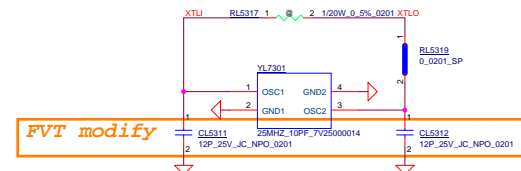
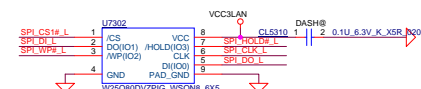
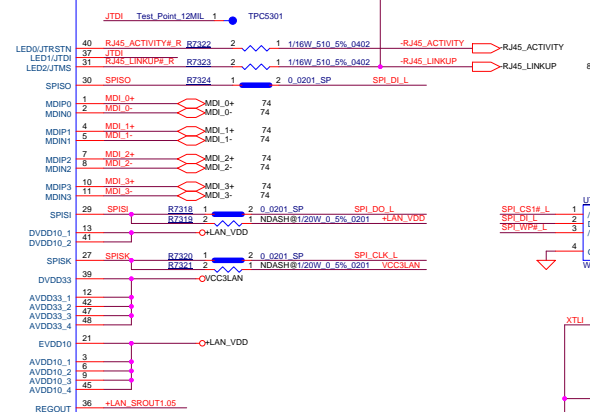
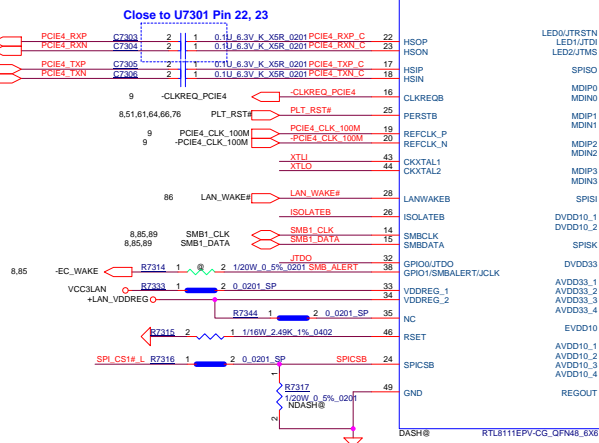
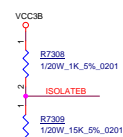
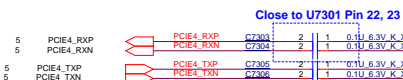
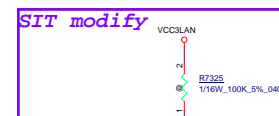
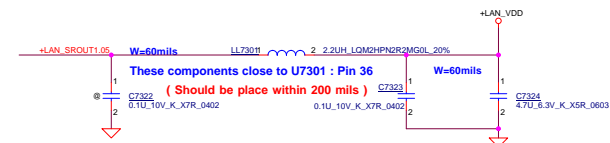
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SMART CARD CONN.

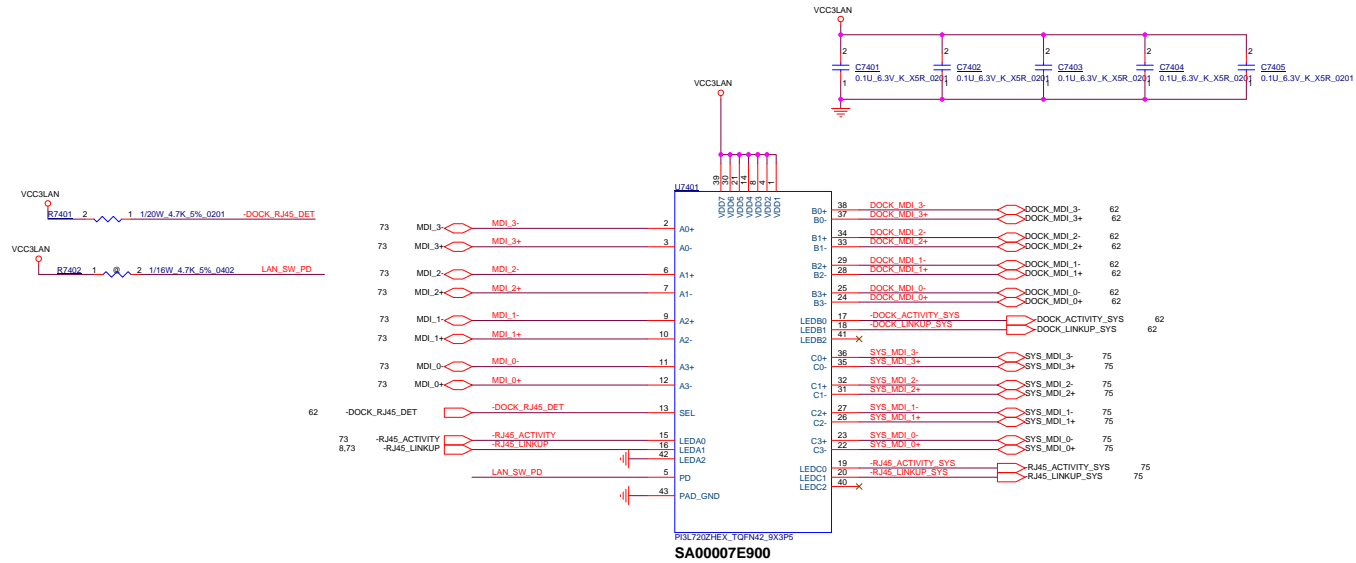


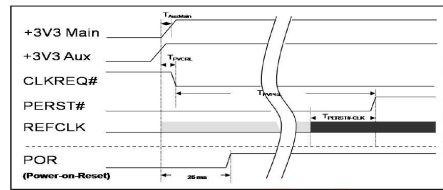
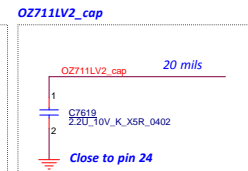
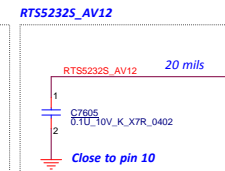
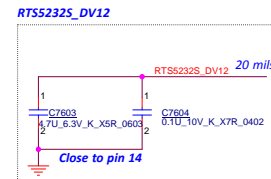
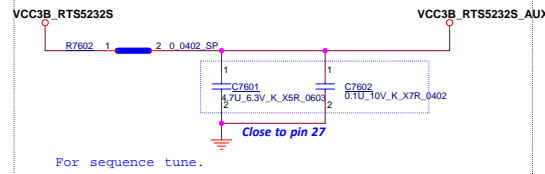
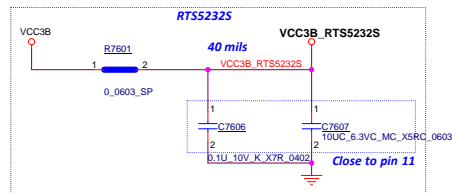


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R7313	X	V

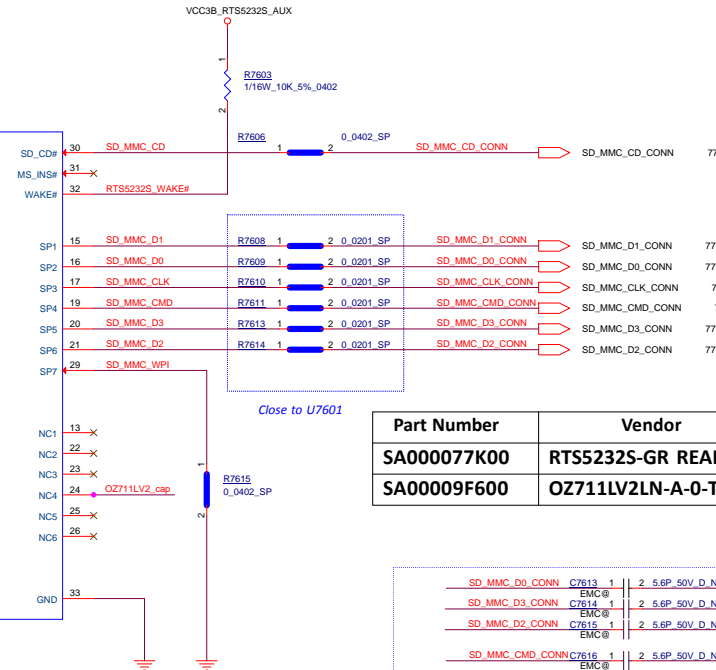
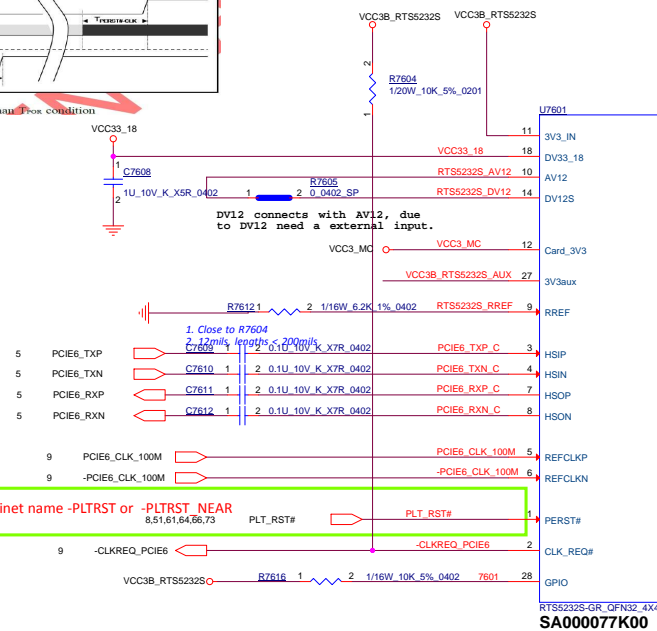


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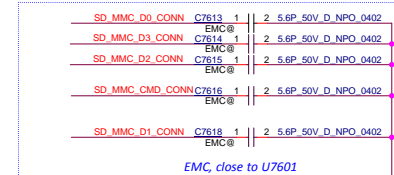


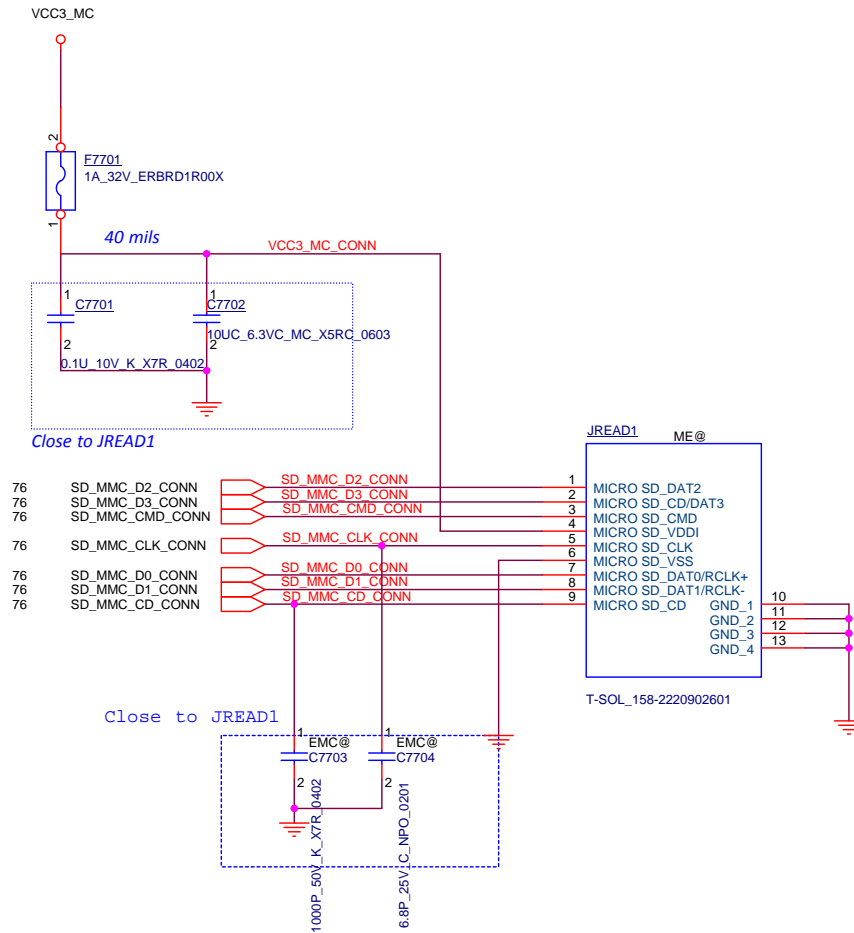


(1) Typical more than 100ns condition.



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SA00009F600	OZ711LV2LN-A-O-TR

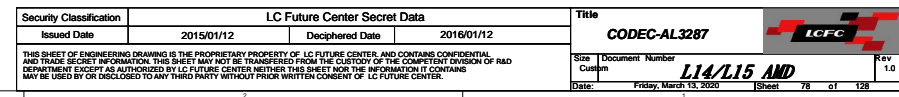




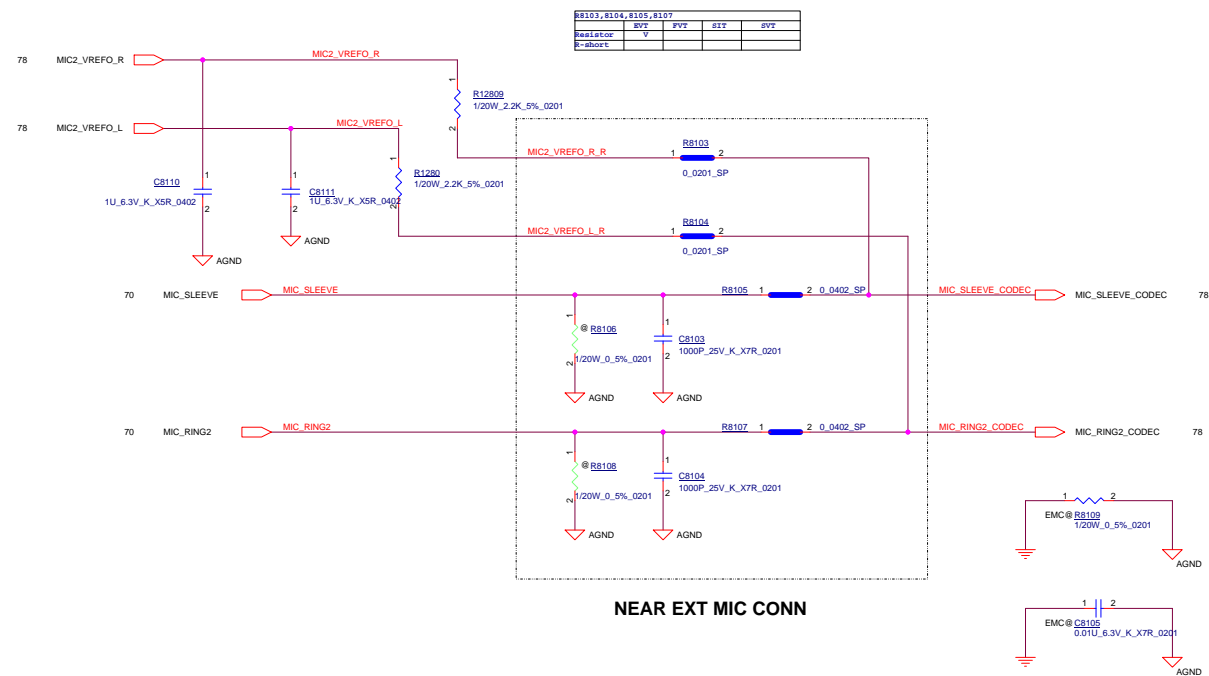
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Card Insert	open

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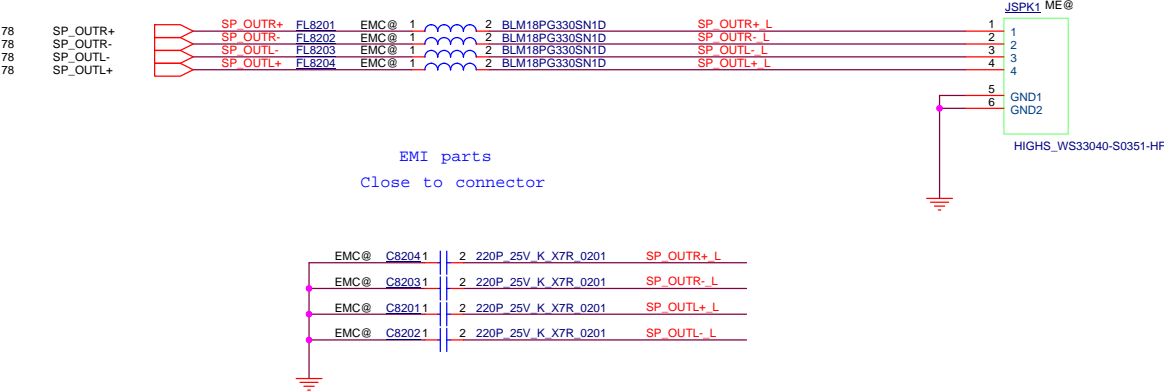
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Date:	Friday, March 13, 2020	Sheet 80 of 128	




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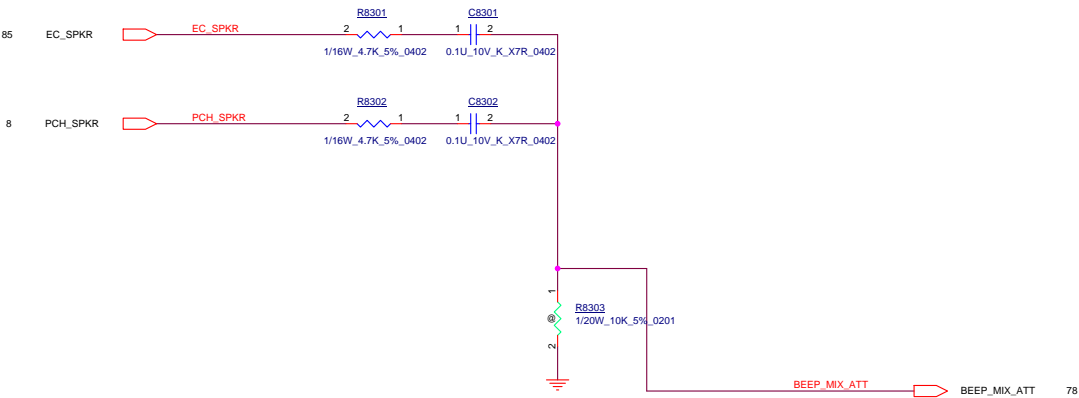
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Issued Date	2018/03/26	Deciphered Date	2019/06/01	AUDIO CONNECTOR	
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SPK CONN.



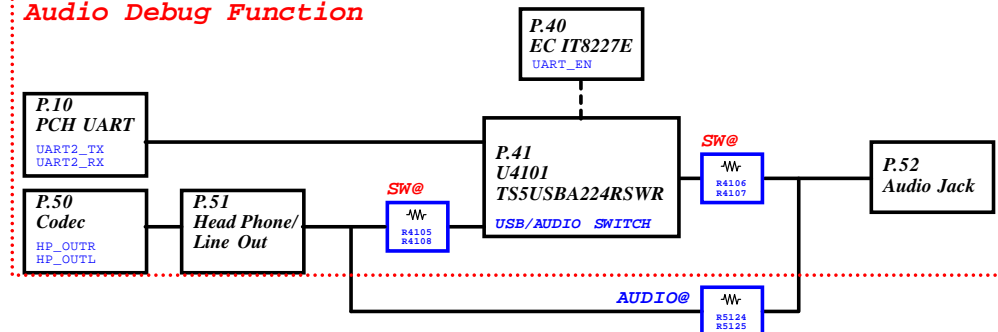
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Issued Date	2018/03/26	Deciphered Date	2019/06/01	AUDIO JACK SENSE		
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Audio Beep

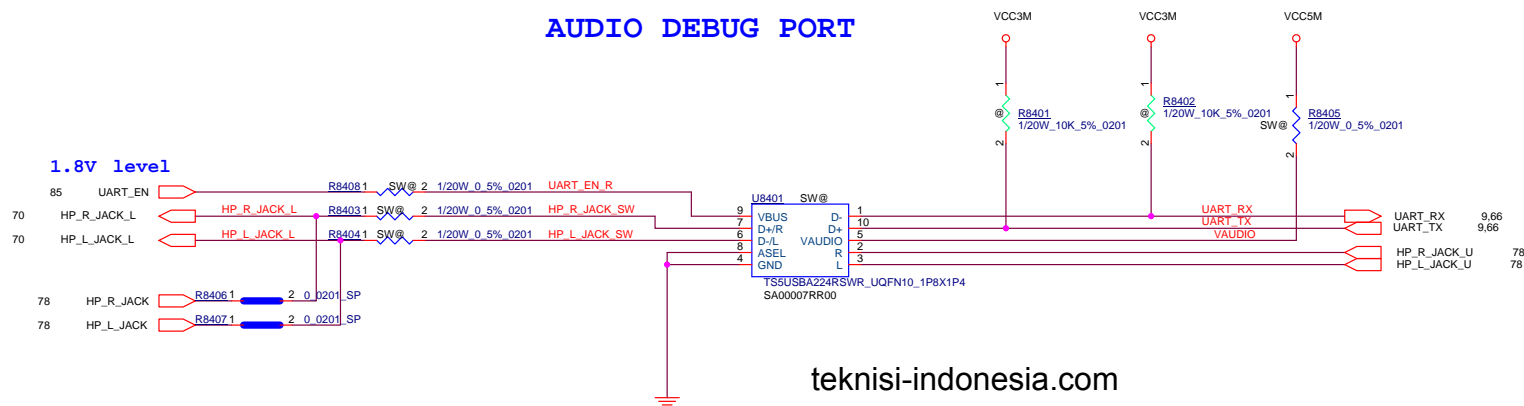


A _{SEL}	V _{AUDIO}	V _{BUS}	L,R	D+, D-
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF ⁽¹⁾	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

Audio Debug Function

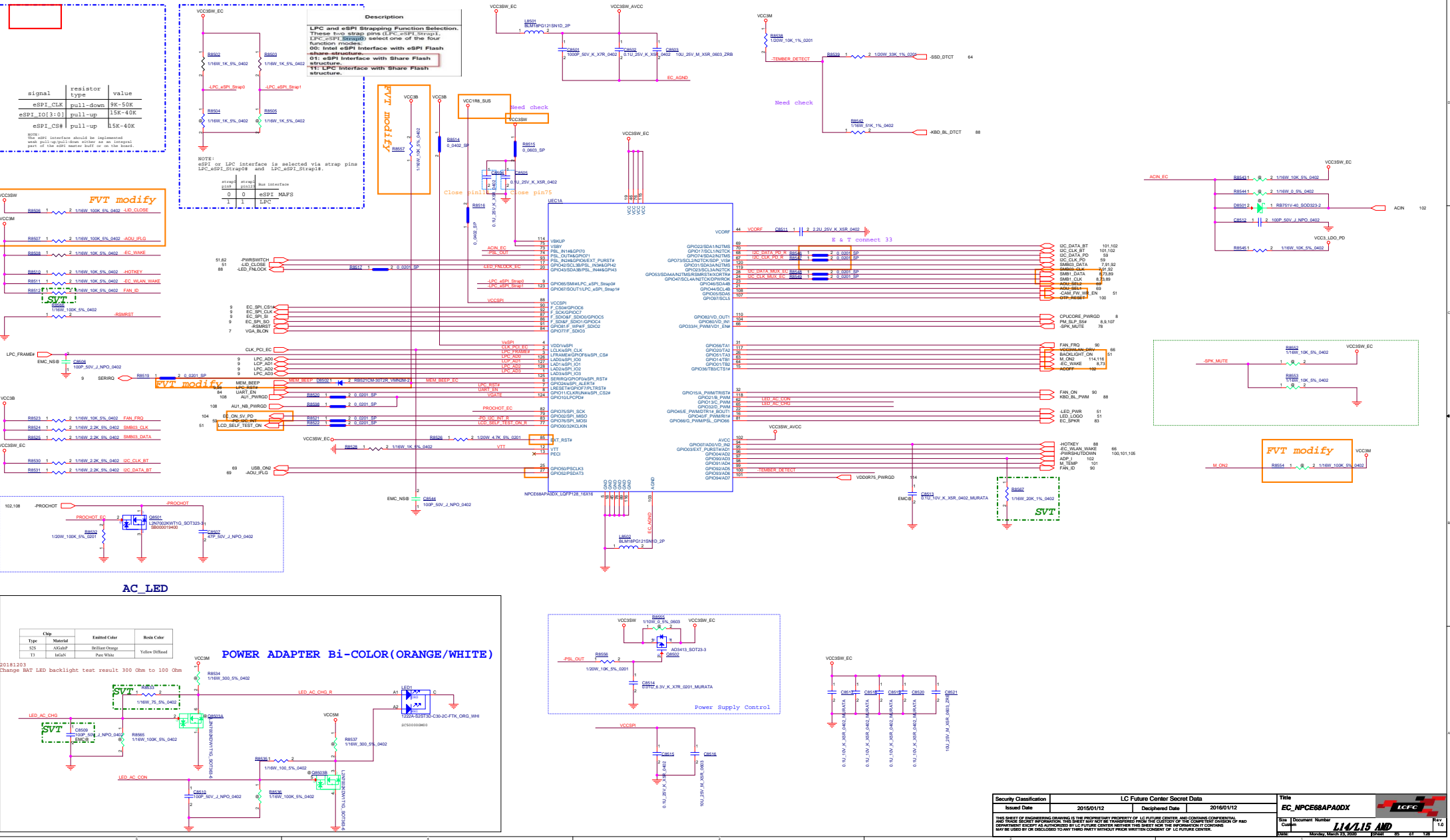


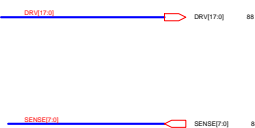
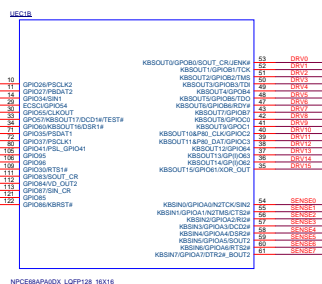
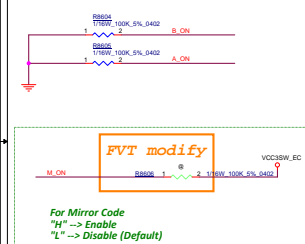
AUDIO DEBUG PORT




Mode	Audio	UART
UART_EN	L	H


Part Name	For NPI	For MP
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R8403 SW@	ASM	NA
R8404 SW@	ASM	NA
R8401 SW@	ASM	NA
R8402 SW@	ASM	NA
R8405 SW@	ASM	NA
R8506 AUDIO@	NA	ASM
R8507 AUDIO@	NA	ASM



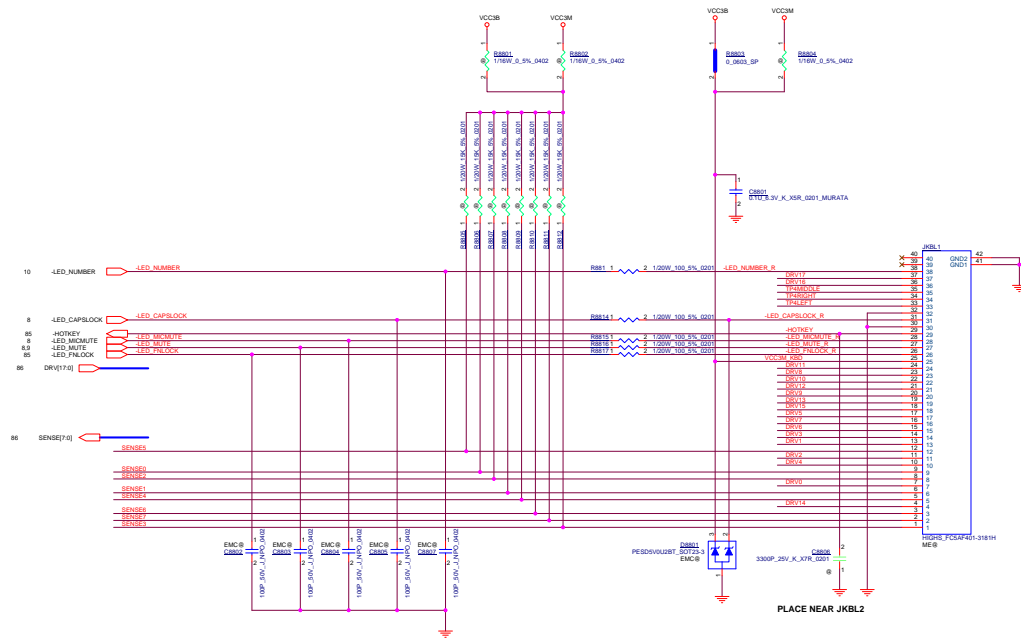


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Keyboard CONN



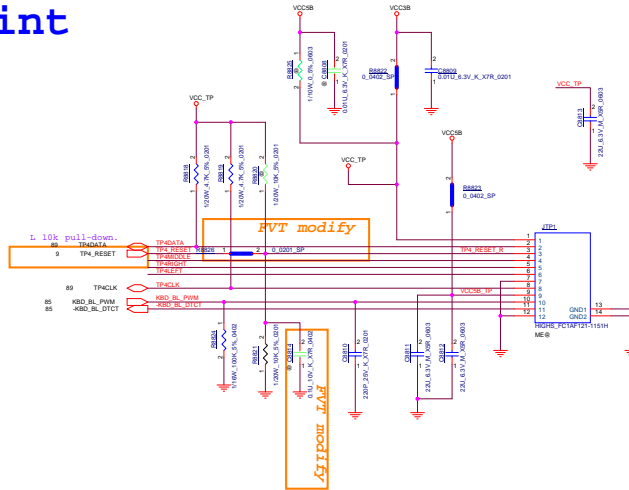
Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for FnLk
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLk
LED5	LED for NumLock
Assign	Purpose
MC	Common pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button

Pin #	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV10
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

Track Point

TrackPoint and Backlight FPC Pin Assignment

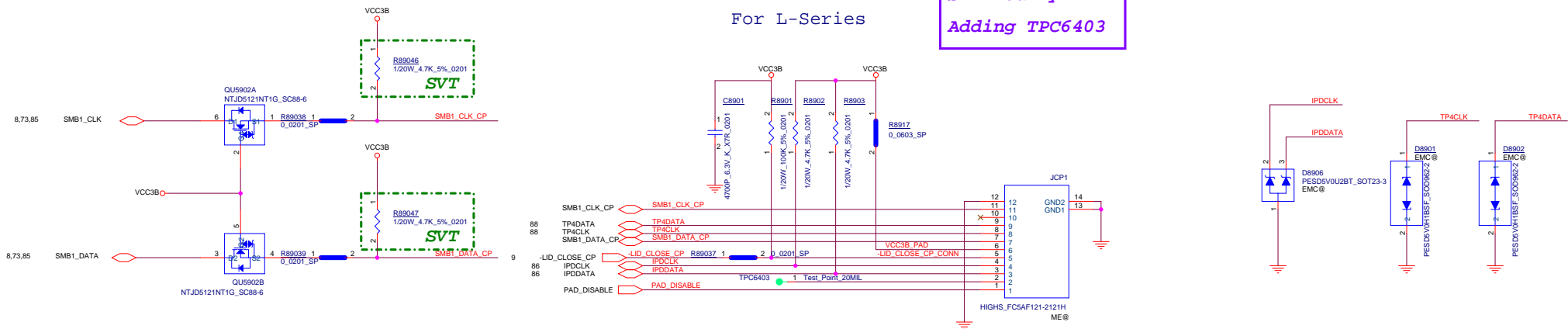
Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	Backlight detection
12	LED GND



Click Pad

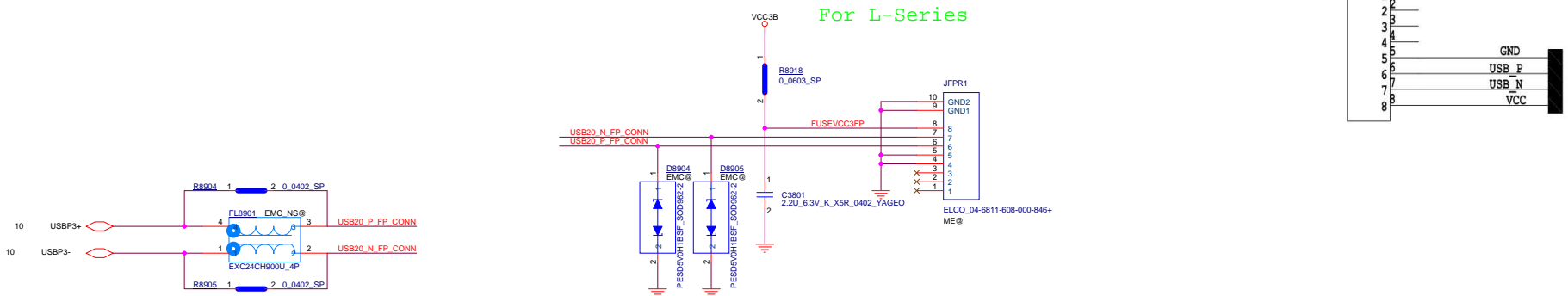
For L-Series

SIT modify
Adding TPC6403

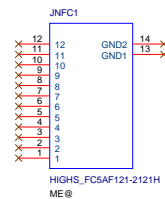


FingerPrint Conn

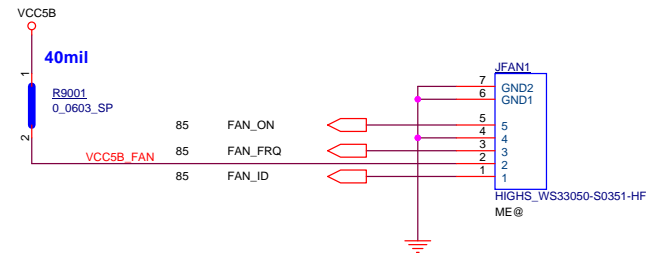
For L-Series




NFC



FAN CONN.



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						Date:	Friday, March 13, 2020	Sheet 90 of 128

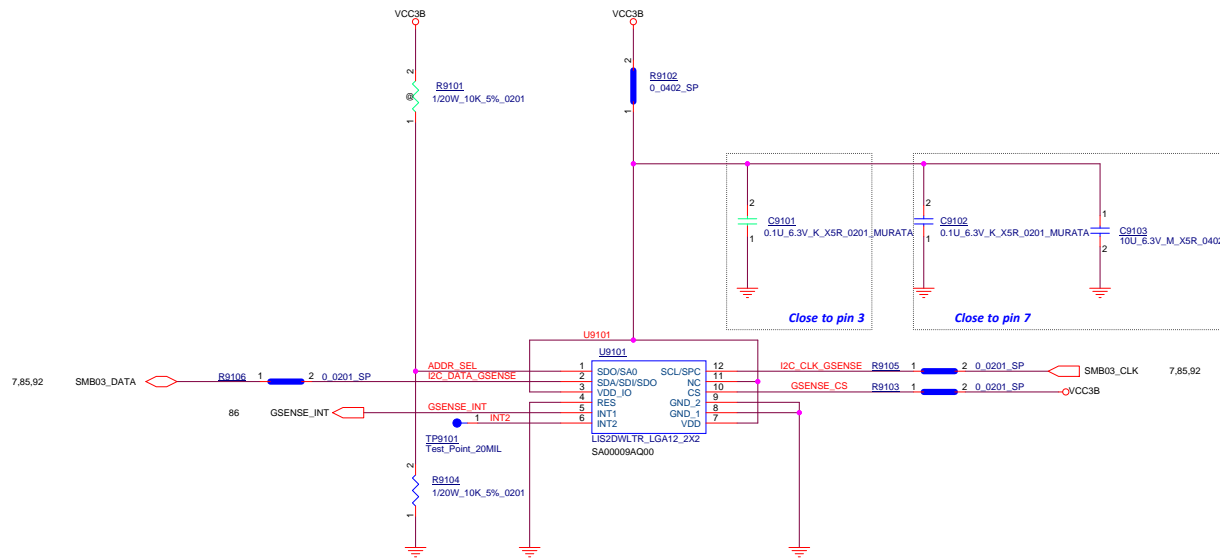
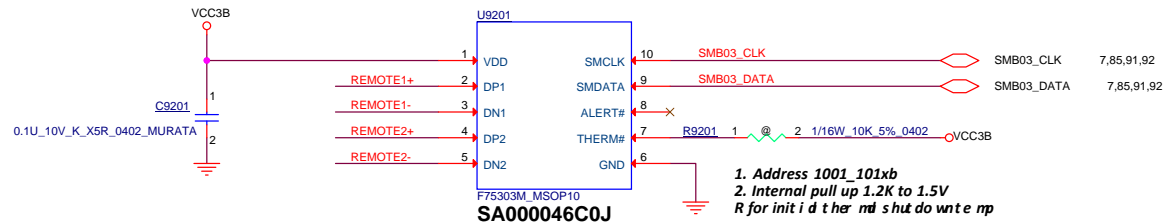


TABLE of G-Sensor (U9101)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
BOSCH	BMA280	SA0000A1600

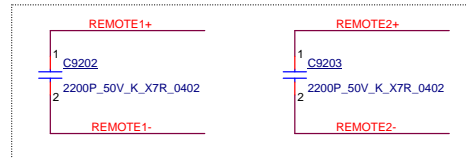
TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
BMA280	H	32h(W),33h(R)
	L	30h(W),31h(R)

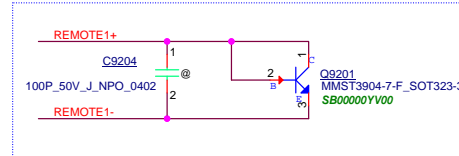
Thermal Sensor Close to CPU



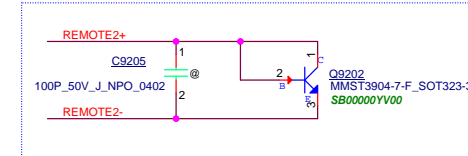
Close to U9201



Close to CHARGER



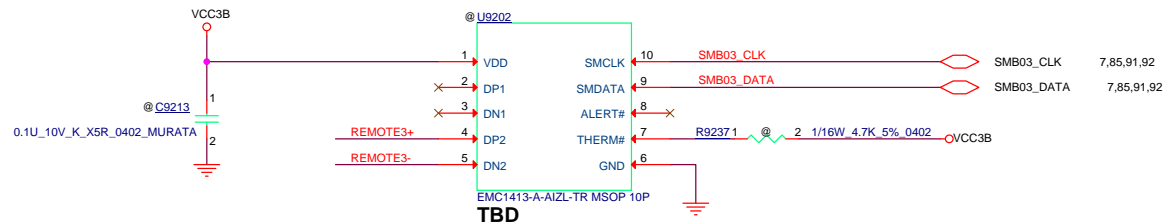
Close to GPU



Trace width/space:10/10 mil
Trace length:<8"

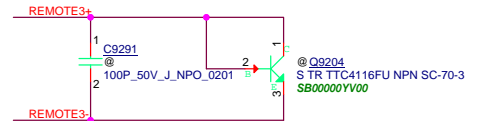
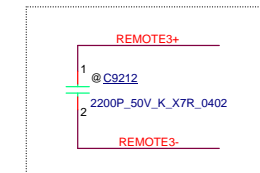
FVT modify

Thermal sensor placed near APU



The SMBus address is 1111_100(r/w)b.


Close to U9202



REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

Security Classification	LC Future Center Secret Data		Title	Thermal Sensor	
Issued Date	2019/03/01	Deciphered Date	2019/07/23		
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				Sheet		95 of 128		

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Issued Date		2019/03/01	Deciphered Date		2019/07/23	
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				Sheet		96 of 128

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Date: Friday, March 13, 2020						Sheet 97 of 128			

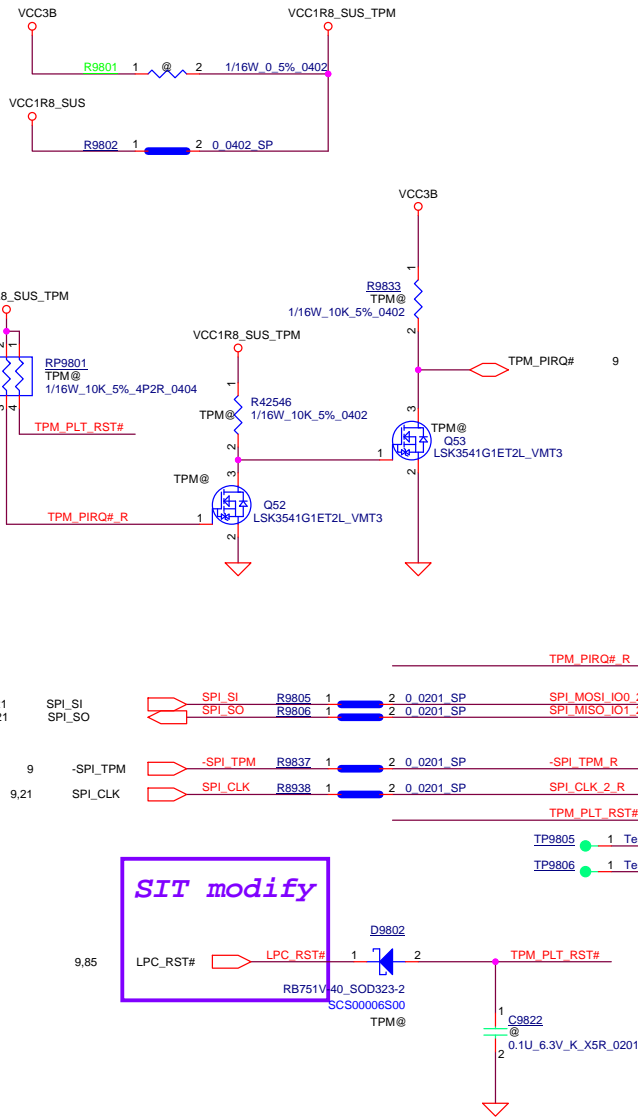
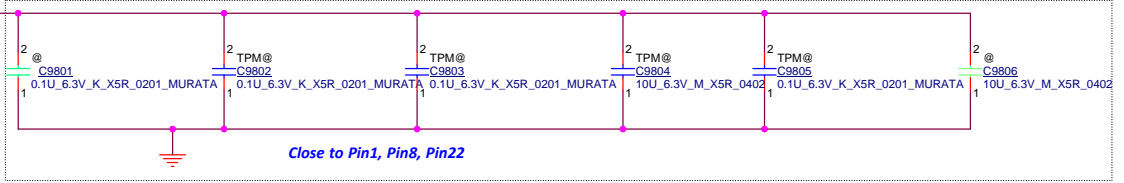
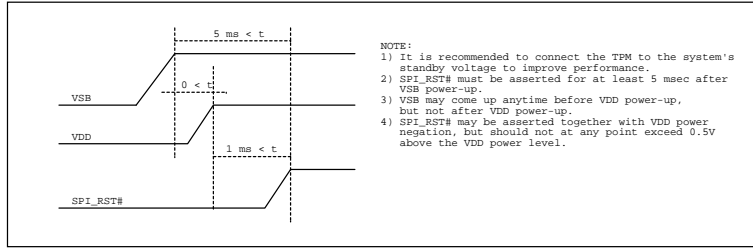


TABLE of TPM (UT5801)		
Vendor	LCFC P/N	Description
NUVOTON	SA00008KS20	S IC NPCT750LADYX QFN 32P TPM 2.0
ST	SA0000AB710	S IC ST33HTPH2X32AHD4 VQFN 32P TPM 2.0


20180730
ST TPM change PN

NOTE:
Check timing sequence in SDV phase.



TABLE

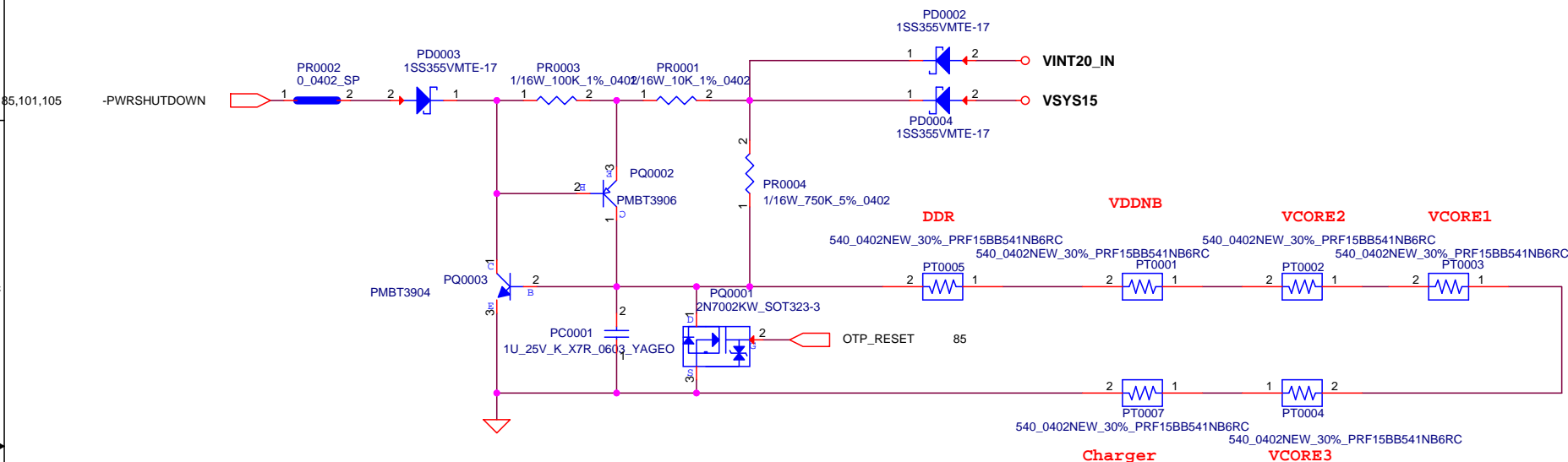
Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HTPH2E32AHC0
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	NC	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC

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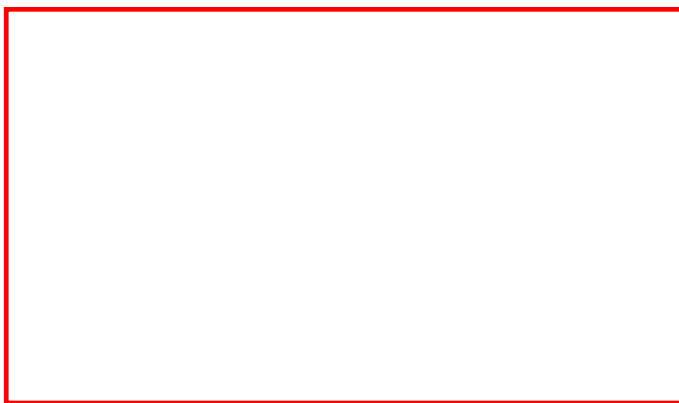
For ME GND hole Screw Hole





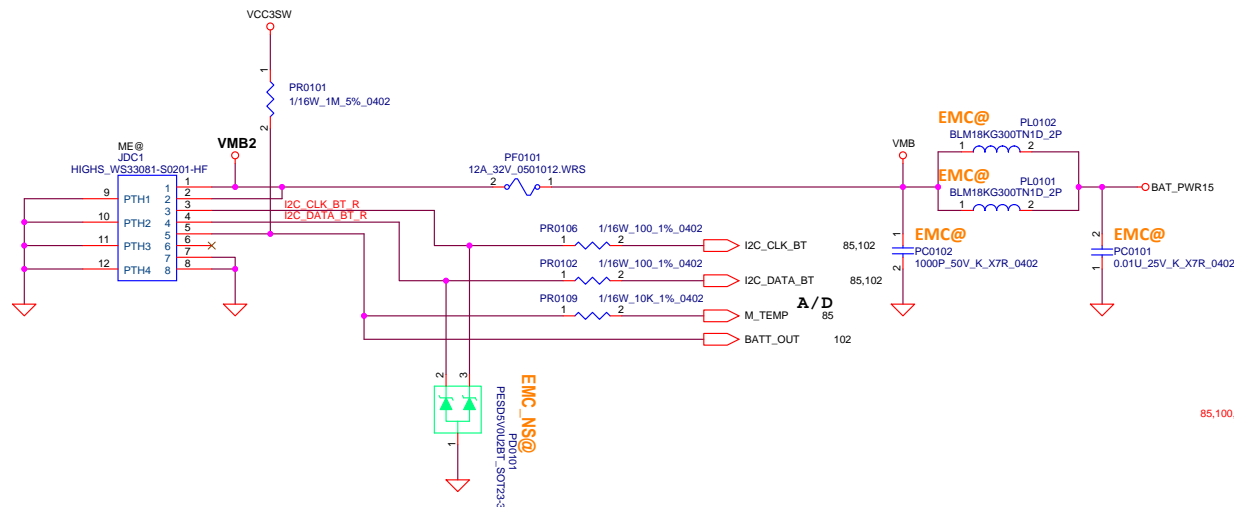
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VINT20_IN
VSYS15 51,102,103,104,105,106,108,109,110,114,116,128
VSYS15
VCC3SW 20,51,59,85,101,102,105,127
VCC3SW



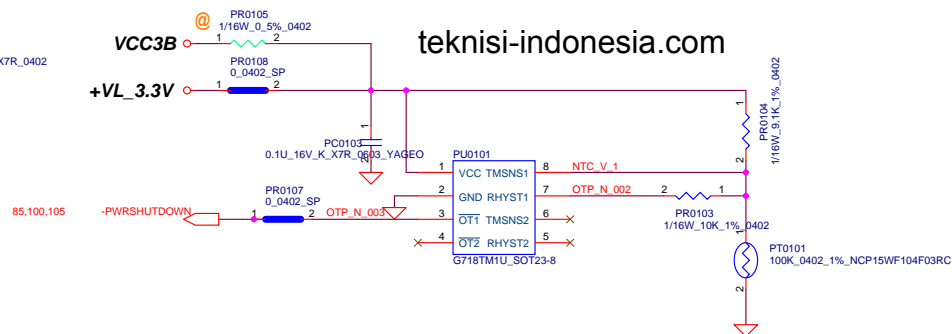
RTC Battery



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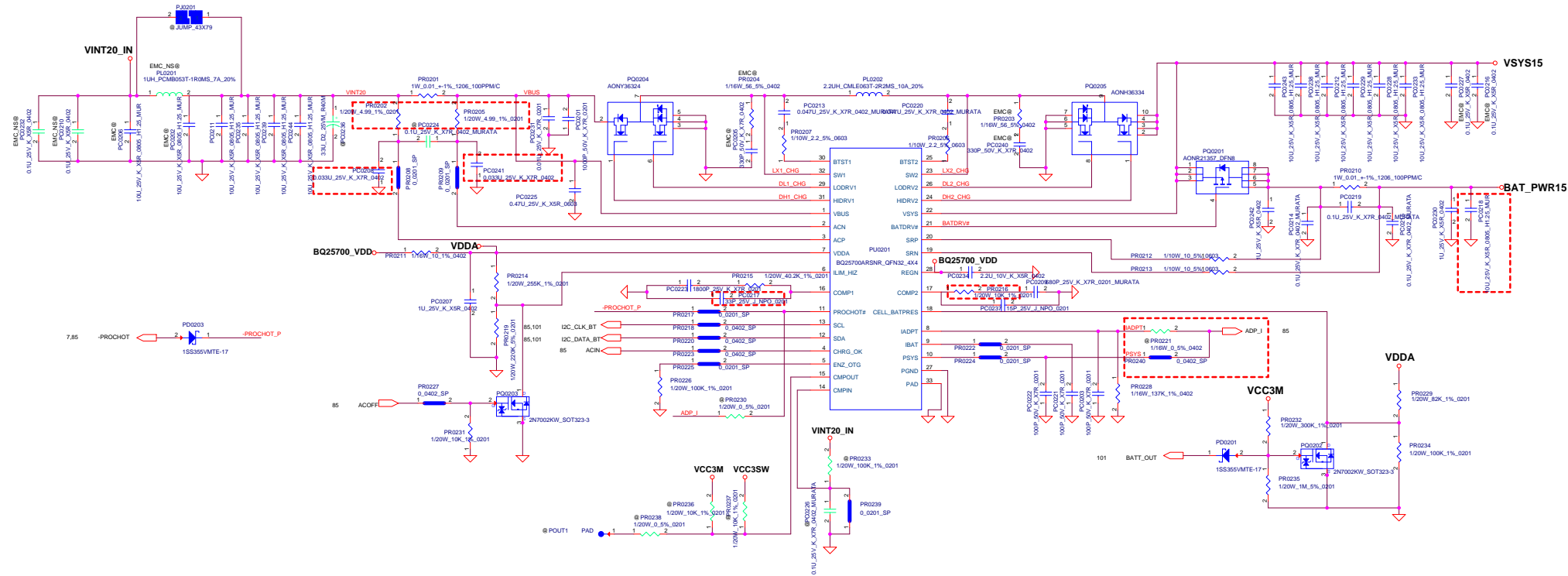


**PRT7 under CPU bottom side for CPU thermal protection.
This is for thermal team request.**

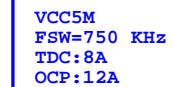


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				Date: Friday, March 13, 2020	Rev 2.0
				Sheet 101	of 128

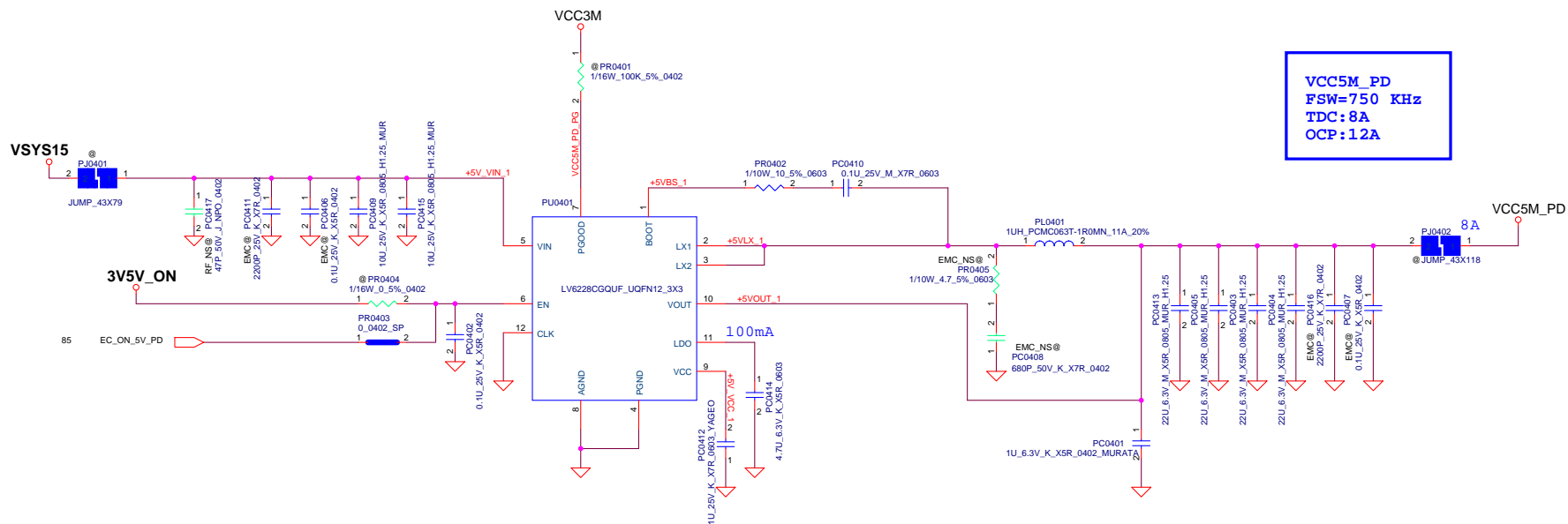
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 BAT_PWR15 101



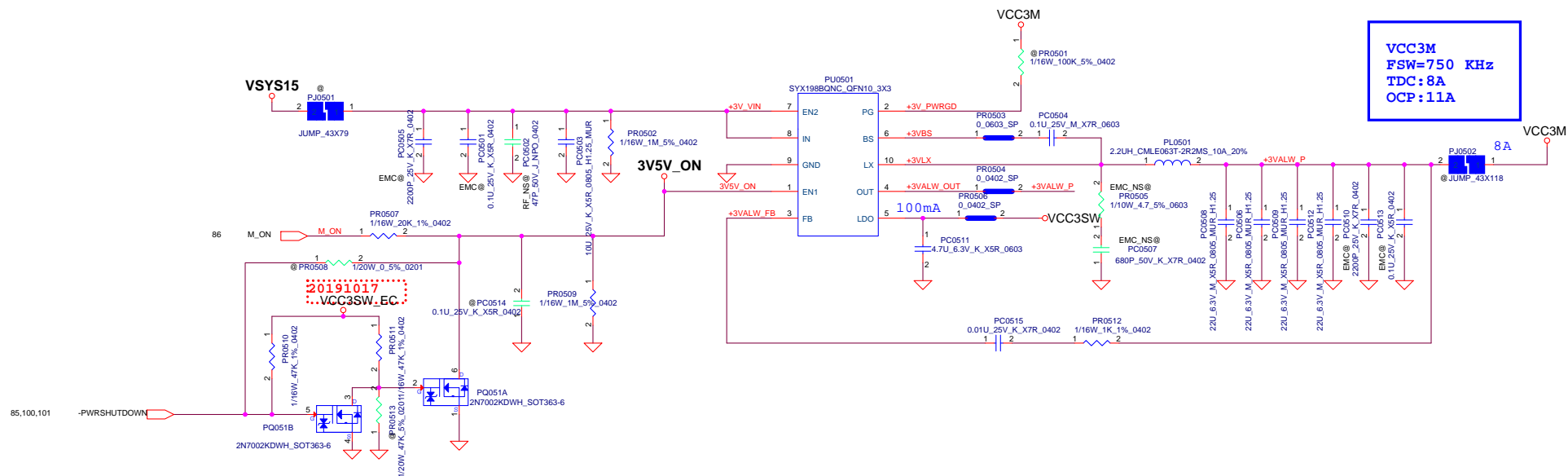
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Issued Date	2013/08/05	Deciphered Date	2014/12/31
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Size	Document Number	Rev	
System	114/L15 AND	2.0	
Date	Friday, March 15, 2020	Sheet	102 of 128

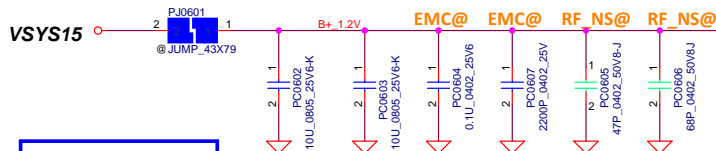


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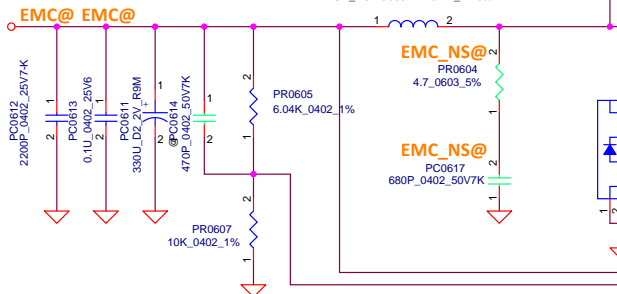




1.2V
TDC: 12A
OCP: 16A
Fsw: 300KHz

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VCC1R2AP



86,107

A_ON

1

2

PR0613

0_0402_SP

1

2

@PR0611

47K_0402_5%

1

2

@PC0619

0.1uF_0402_16V

1

2

@PC0618

0.1uF_0402_6.3V7-K

1

2

PR0612

0_0402_SP

1

2

B_ON

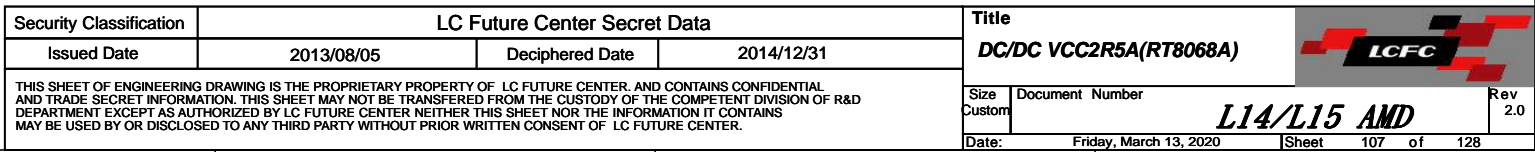
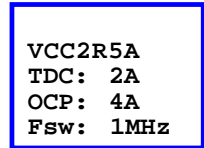
78,86,127,128

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Custom			2.0
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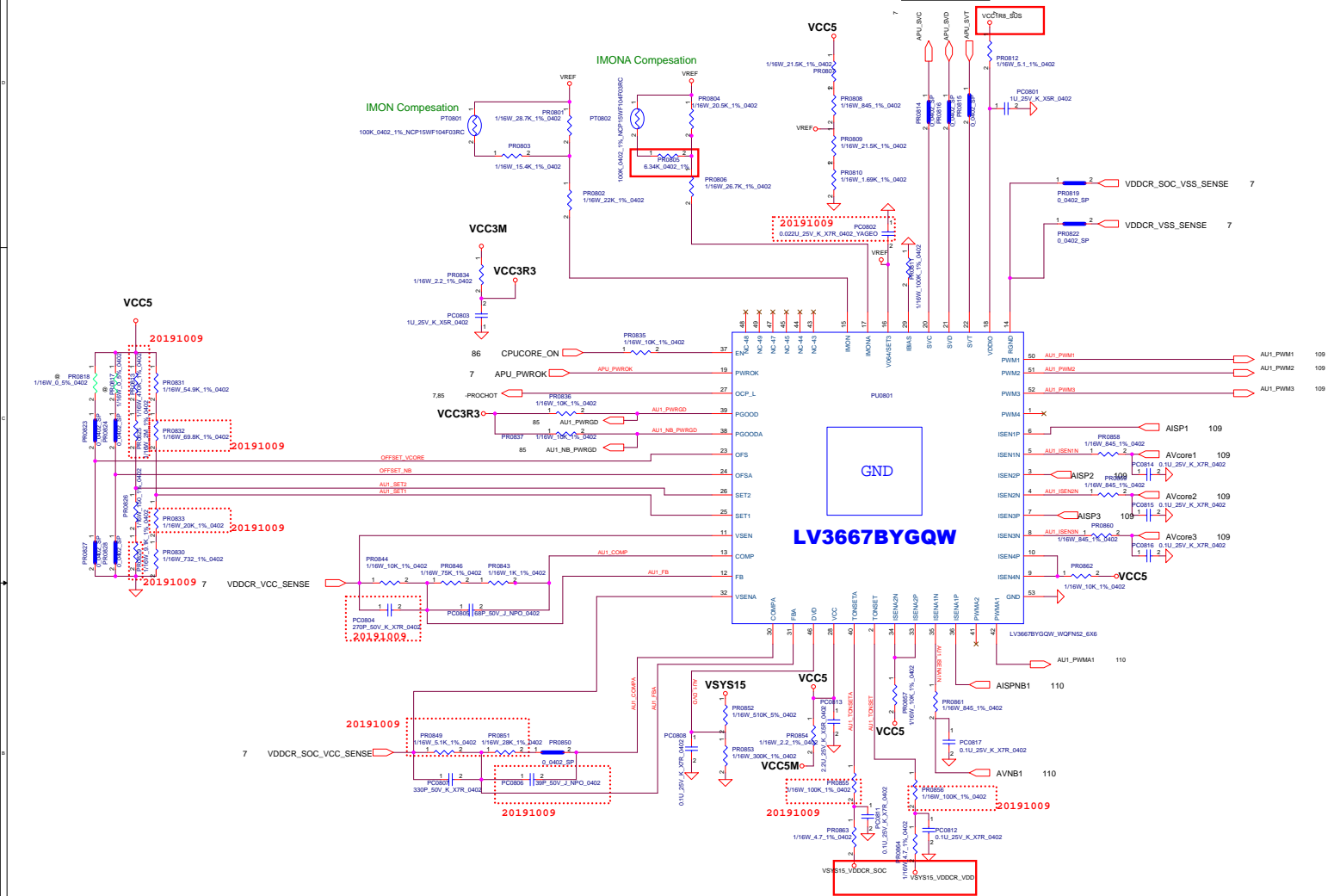


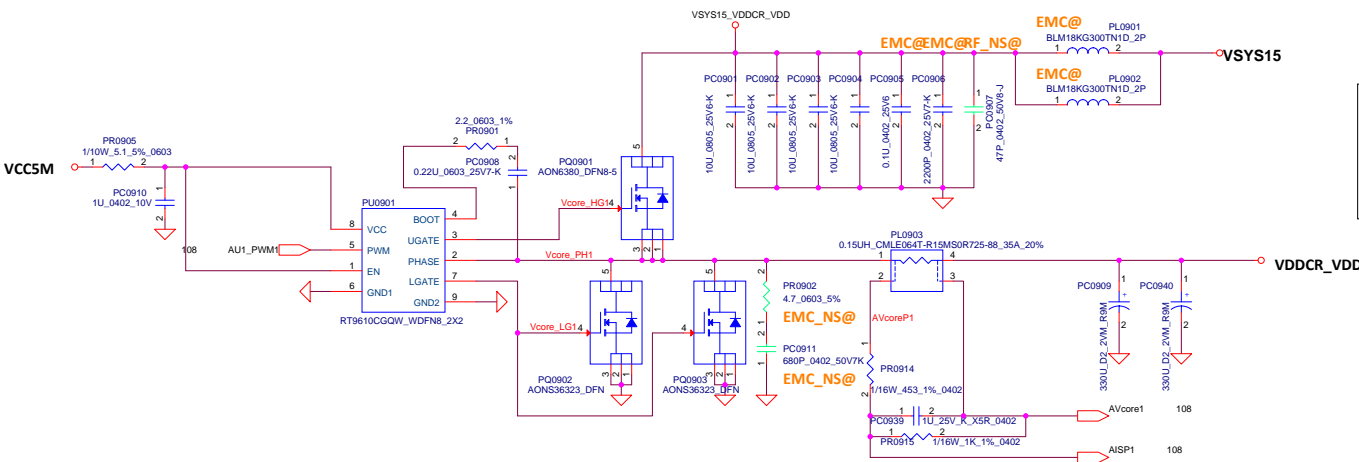
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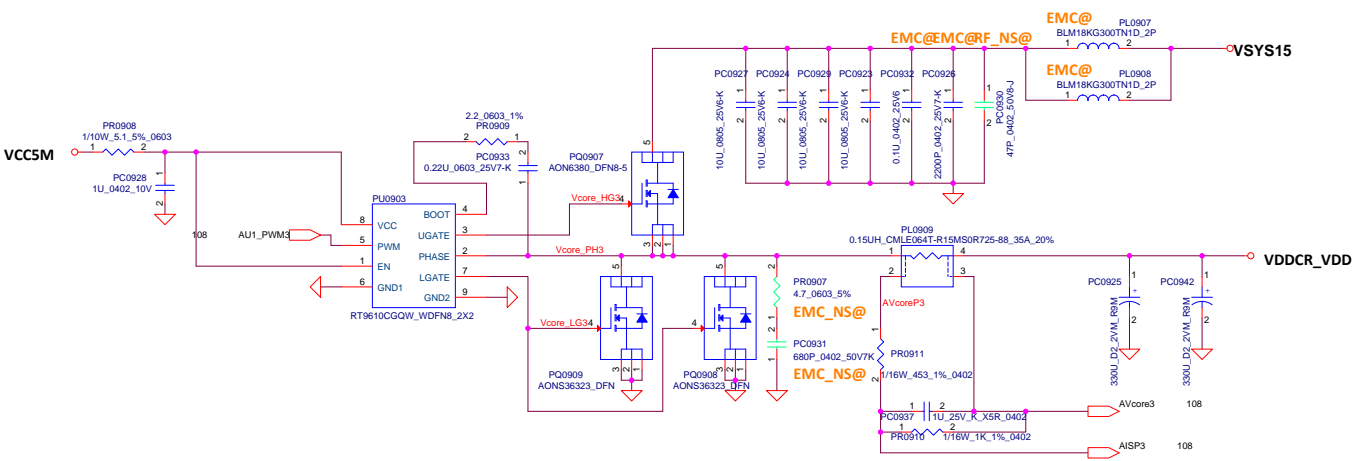
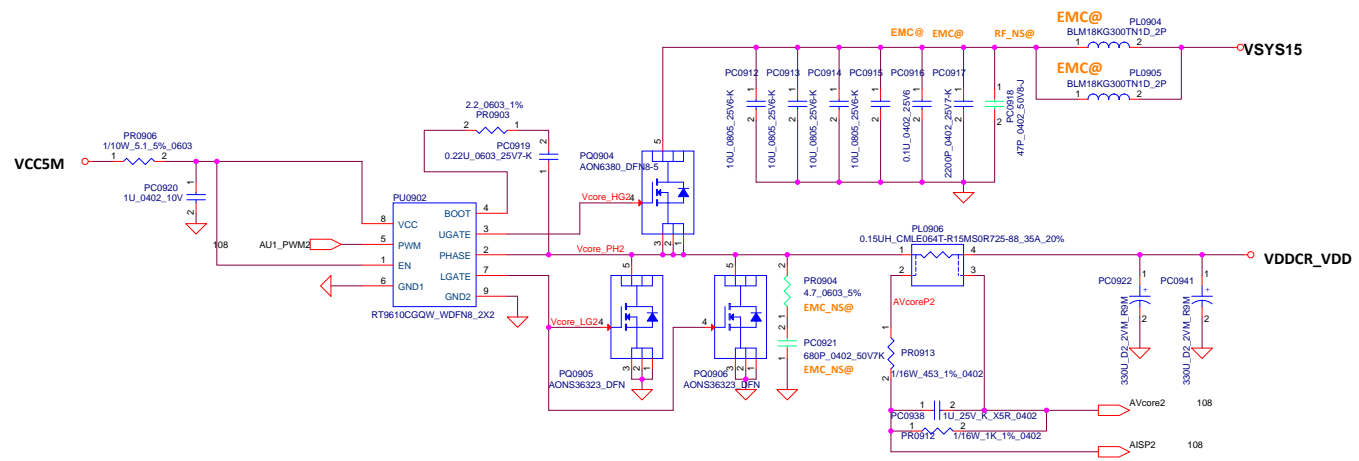
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VCC5M 51,69,70,84,85,103,106,107,109,110,114,116,128

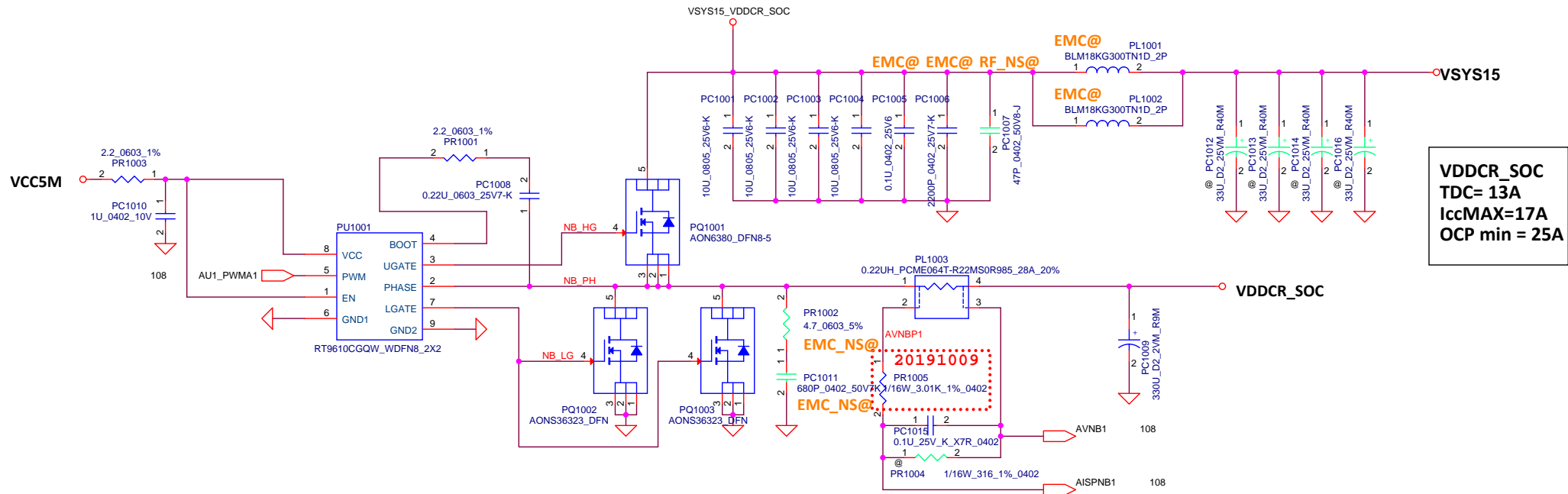
Boot-VID		
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V







For VDDCR_VDD
VCCPUCORE
TDC= 44A
IccMAX=70A
OCP=98A

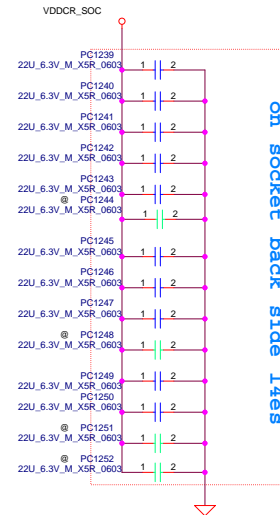
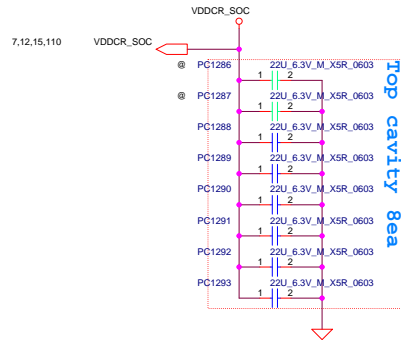
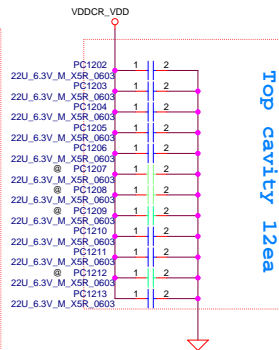
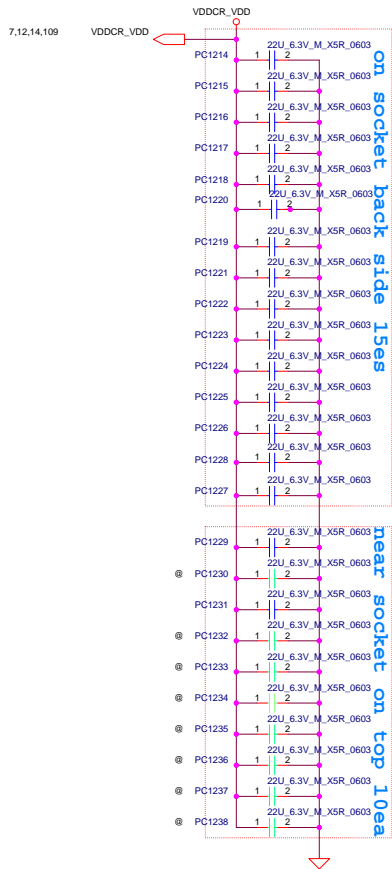




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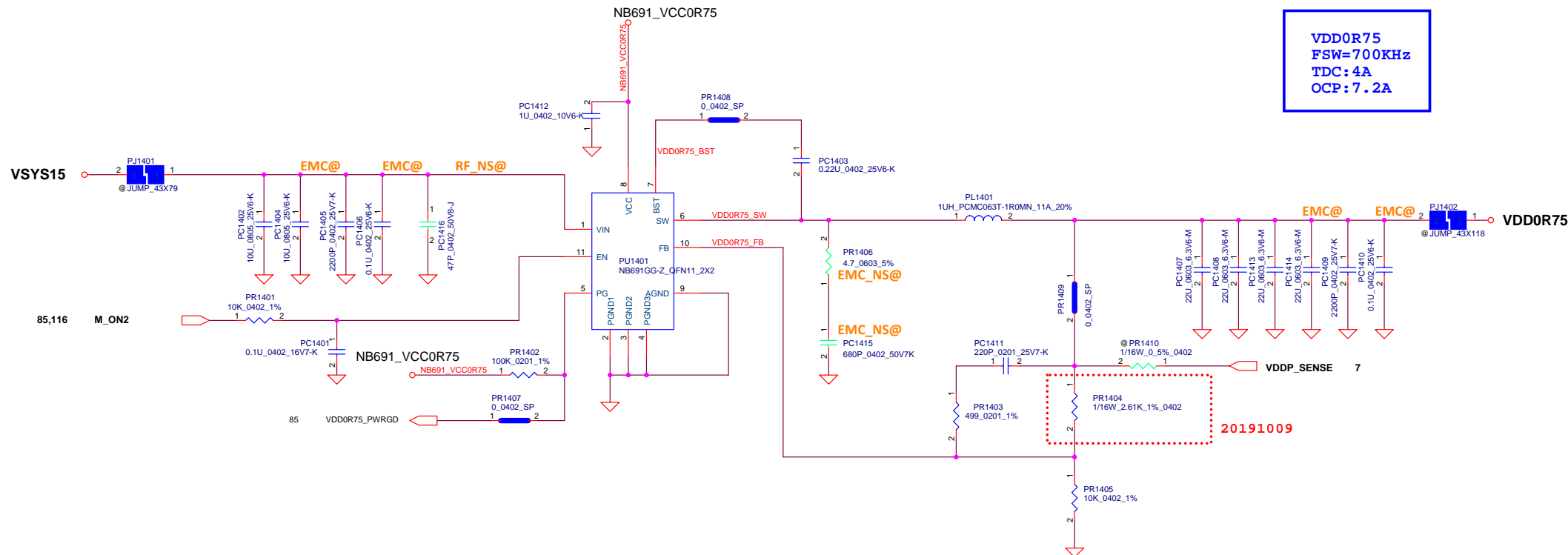
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VSYS15 VSYS15 51,100,102,103,104,105,106,108,109,110,116,128

VCC1R35VIDEO VCC1R35VIDEO



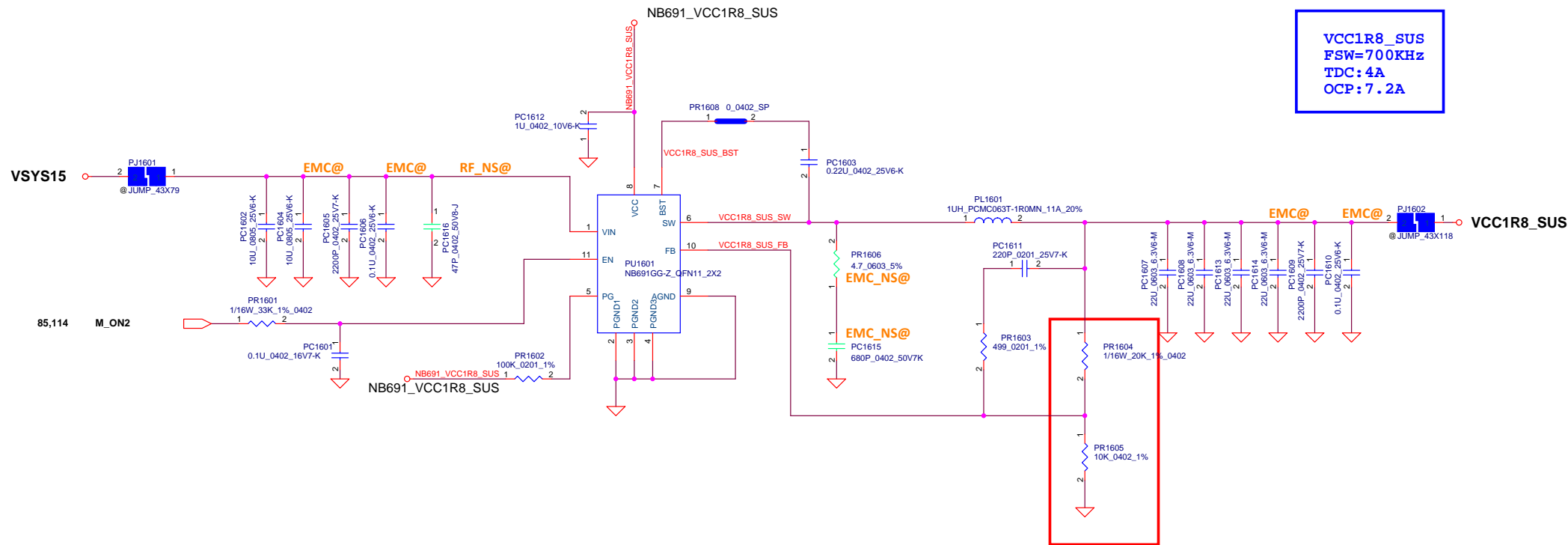
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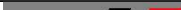
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VSYS15 51,100,102,103,104,105,106,108,109,110,114,128

VCC1R35VIDEO



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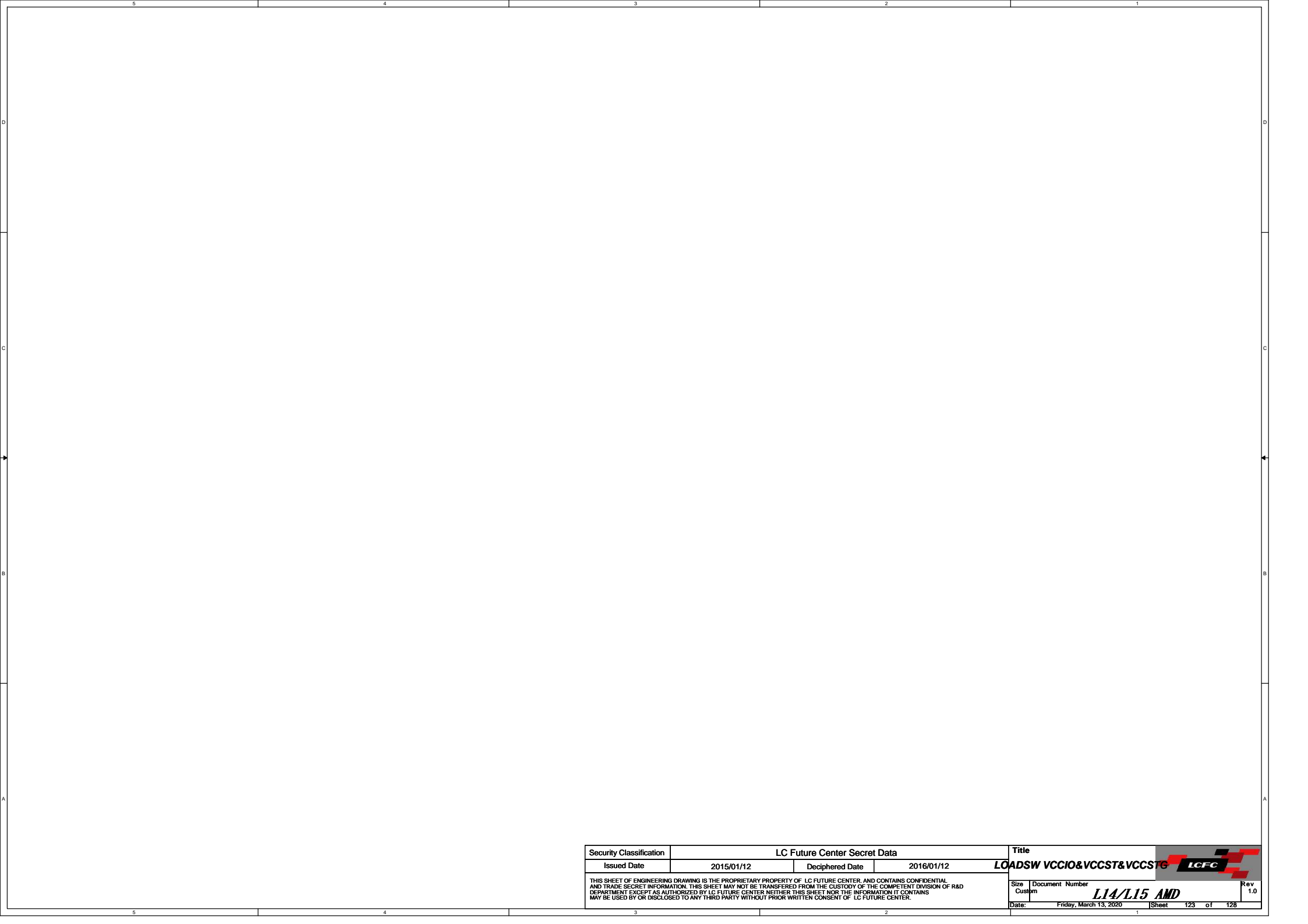
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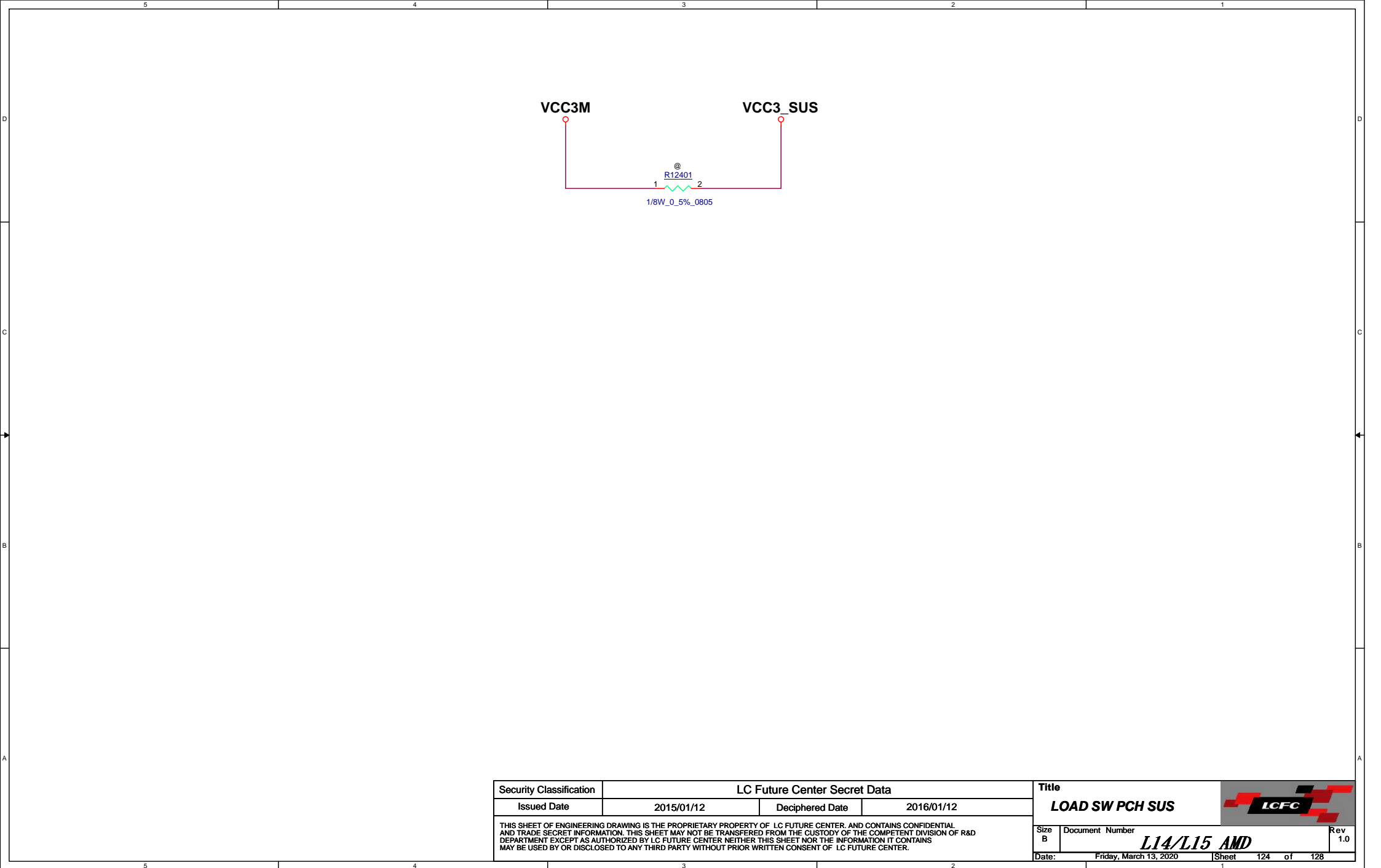
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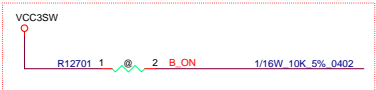
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<table><tr><td colspan="2">Security Classification</td><td colspan="2">LC Future Center Secret Data</td><td rowspan="2">Title</td><td rowspan="2"></td></tr><tr><td>Issued Date</td><td>2015/01/12</td><td>Deciphered Date</td><td>2016/01/12</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>Size B</td><td>Document Number</td></tr><tr><td colspan="4"></td><td colspan="2">L14/L15 AMD</td></tr><tr><td colspan="4"></td><td>Date:</td><td>Friday, March 13, 2020</td></tr><tr><td colspan="4"></td><td>Sheet</td><td>126 of 128</td></tr></table>					Security Classification		LC Future Center Secret Data		Title		Issued Date	2015/01/12	Deciphered Date	2016/01/12	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size B	Document Number					L14/L15 AMD						Date:	Friday, March 13, 2020					Sheet	126 of 128
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VCC3SW		VCC3SW	20,51,59,85,101,102,105
VCC3M		VCC3M	7,8,9,10,12,23,51,59,62,63,66,73,84,85,86,88,102,103,104,105,108,124
VCC5M		VCC5M	51,69,70,84,85,103,106,107,108,109,110,128
VCC5B		VCC5B	51,54,72,78,88,90
VCC3B		VCC3B	7,8,9,12,23,33,35,51,54,57,58,59,61,64,67,70,73,76,78,85,88,89,91,92,98,101,106



1. MIRROR code, is correct????
2. After reset EC, EC control "Low", not High or Disable.

Smart Switch
VCC5M To VCC5B
VCC3M To VCC3B

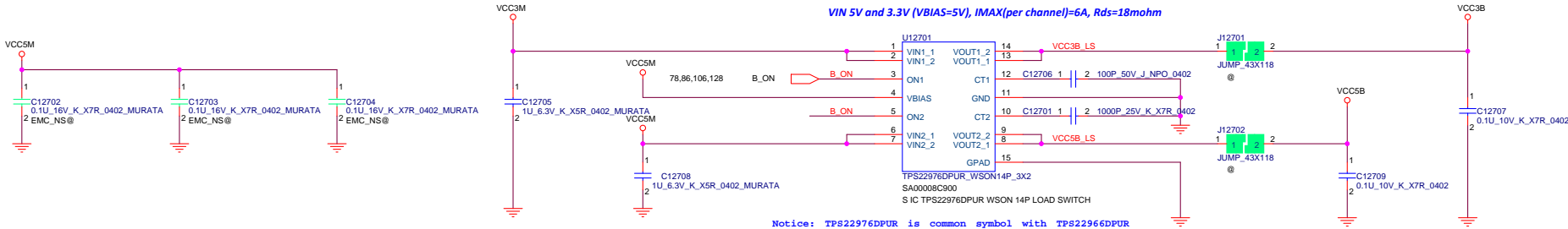



TABLE of POWER SWITCH (U7201)		
Vendor	LCFC P/N	Description
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GMT	SA00008F400	S IC G2898KD1U TDFN 14P LOAD SWITCH

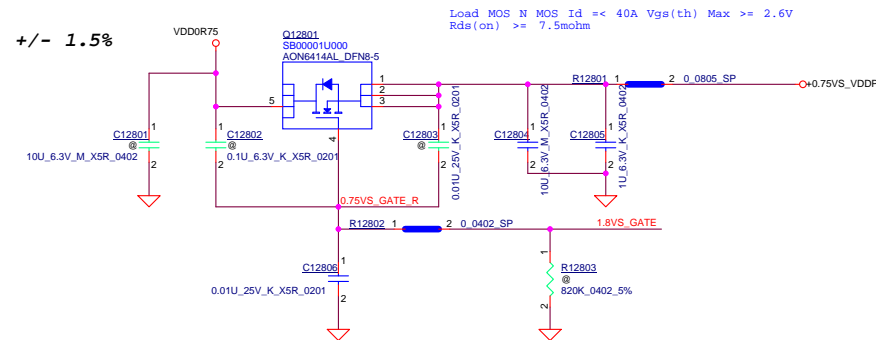
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+VDDP load Switch

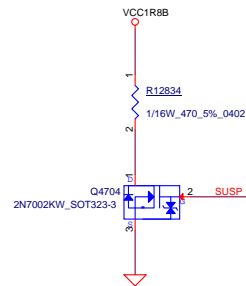
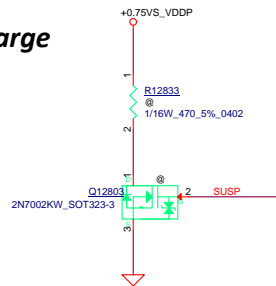
VDD0R75 to +0.75VDDP 10A request

V9B+

9V--13V



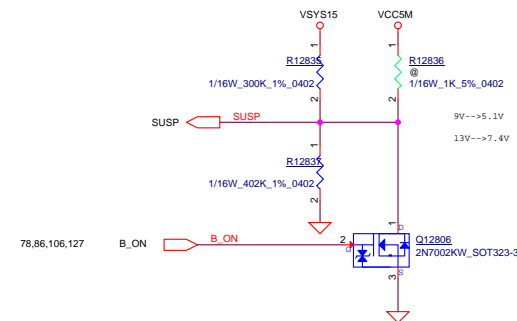
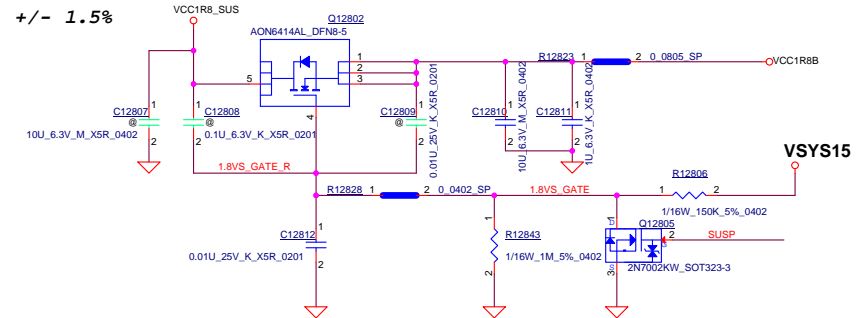
For DisCharge




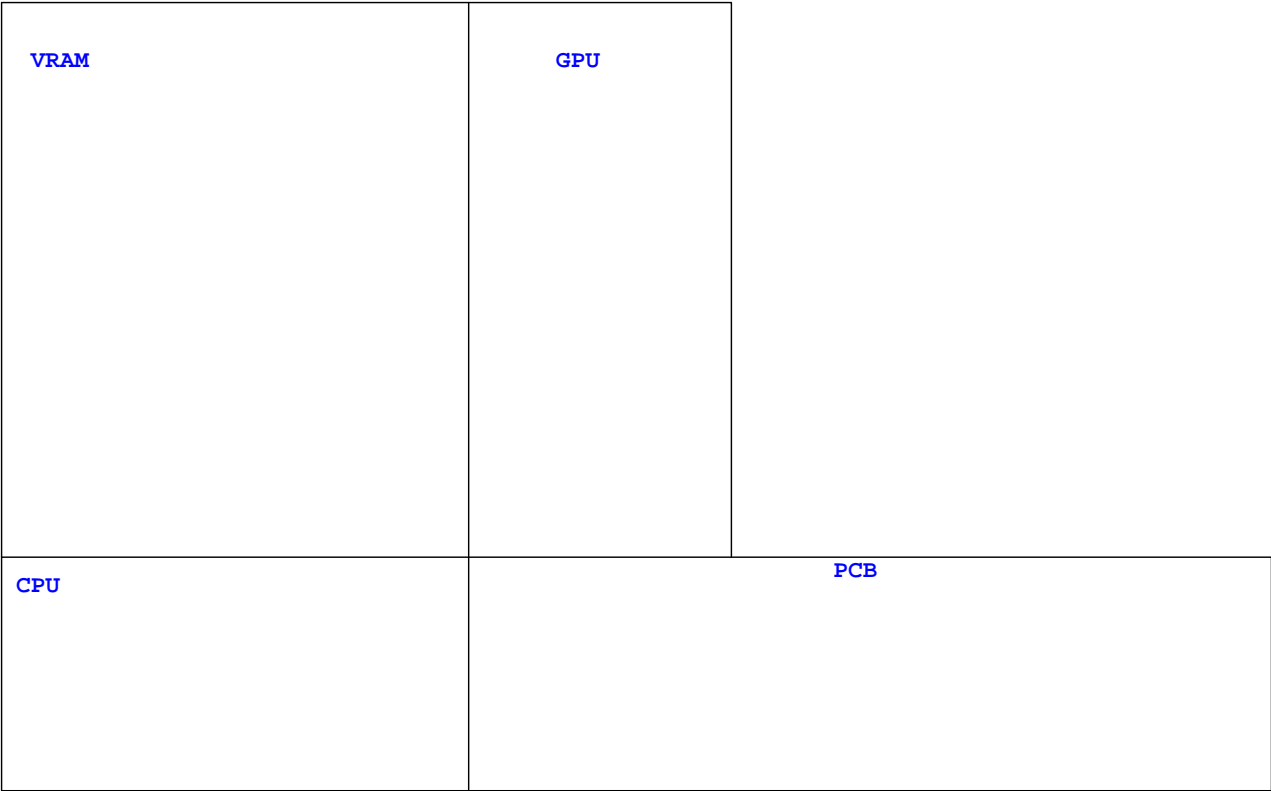
VCC1R8B load Switch VCC1R8_SUS to VCC1R8B 2.7A request


Load MOS N MOS Id =< 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

+/- 1.5%



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